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(54) Sensor arrays.

(57) A sensor array (12) provides a plurality of distinguishable bitmap images of a pattern (22) and comprises an array of sensor cells (20) capable of sensing radiation. The cells are connected in a manner to form distinguishable bitmap images of a contrasting pattern through a pattern of correspondence among the cells. Each bitmap image formed comprises a combination of one or more cells which have responded to the incidence of radiation within a field of array cells that have either not responded or been inhibited from responding. The pattern of correspondence may be one of inhibition or of response of sensors. The patterns of correspondence create bitmap images. The variations between successive bitmap images give a measure of the direction and amount of movement of the sensory array relative to the pattern, which can be used to control the movement of a cursor over a computer display screen.

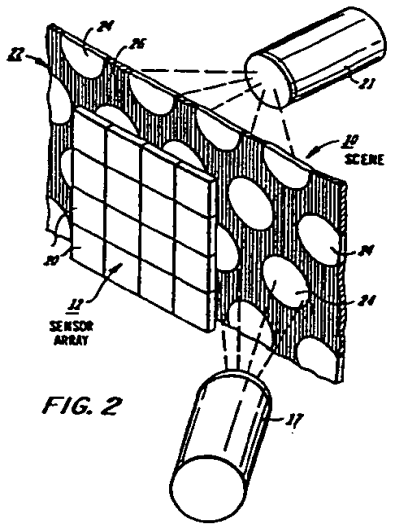


FIG. 2

./...

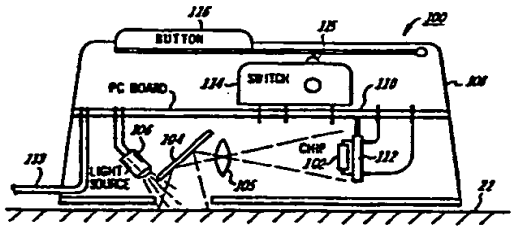

116
BUTTON
115
100
PC BOARD
114
SWITCH
110
108
106
104
CHIP
102
112
LIGHT SOURCE
105
113
22

FIG. 22

SENSOR ARRAYS

This invention relates to sensor arrays and in particular to sensor arrays to perform bitmap functions in digital computing systems and in applications for such systems, such as cursor control devices.

Over the past decade or so, the functional control device for use, for example, with a computer display system has developed with the development of such systems. These devices have taken several forms, such as joy sticks, light pens, touch panels and hand held cursor control devices, now also referred to as a "mouse". One of the most prevalent uses of these devices is to alter the display at selected locations on a visual display of such systems by controlling a display cursor which is selectively moved over the display by means of the control device.

The mouse is a pointing device used with interactive display oriented computer systems, particularly to control the cursor on the system display. The mouse tracks the movement of a user's hand as the user moves the mouse about on a work surface or pad usually next to the user's keyboard input to the system. Microswitches may be positioned on the top surface of the housing of the mouse to perform various functions in the system upon finger operation of a switch selected by the user. The mouse device has recently become available in the office products market as a part of the 8010 Professional Workstation, developed, manufactured and distributed by Xerox Corporation.

Research has led many to conclude that the mouse concept is the preferred and best means for performing cursor function controls, some of the reasons being its adaptability for use in conjunction with a keyboard input of such systems from a human engineering standpoint and ease of display cursor movement with desired functions implemented by microswitches present on the mouse. These cursor control devices or "mice" have been known of electromechanical design. Examples of such devices may be found in U.S. Patents 3,304,434; 3,541,541, 3,835,464; 3,892,963 and 3,987,685.

The best known electromechanical and "grandfather" mouse was developed at Stanford Research Institute and is disclosed in Patent 3,541,541. This mouse employs a pair of

wheels that turn potentiometer shafts to encode X and Y m ti n into analog signals. Each wheel turns as the mouse is moved along its respective coordinate direction and slips sideways as the mouse is moved in an orthogonal direction. When the mouse is moved diagonally, both wheels turn and slip simultaneously. The design of this mouse led to the use of ball bearings as wheels and optical shaft encoders to generate a two bit quadrature signalling code, as disclosed in Patent 3,892,963. The motion of a wheel caused a two bit output for a coordinate direction to form square waves in quadrature, with phase and frequency determined the direction and speed of travel. Each bit transition represented motion of one resolvable step which was employed to move the cursor on the display screen. Further development led to the employment of a ball or sphere instead of two wheels for more uniform tracking (Patents 3,835,464 and 3,987,685). Internally, the sphere itself was a trackball with shafts turning against the ball and with commutation as shaft encoders or optical disc encoders, the latter being disclosed in Patent 3,304,434.

While these mice have proved to be quite useful in performing display functions, they have not been outstandingly reliable, particularly over long periods of use. For example, the mechanical moving parts of the mouse, such as the balls and wheels, become dirty and slip on the work surface or pad, rather than provide continuous rolling action, or the commutators become dirty and skip.

Also, because of the precision and tolerances necessary for the mechanical moving parts and the number of parts involved, these mechanical mice have been expensive to fabricate.

The goal, therefore, is to design a mouse with no moving parts (excluding the microswitches) thereby eliminating the above-mentioned mechanical disadvantages and providing a mouse with high reliability over long periods of time. One direction toward the goal of no moving parts is optics and optical detection of mouse tracking functions. The concept of optical tracking, i.e., optical detection of an optical image, such as a track, lines, bars or grating, is not new. Examples of such tracking utilizing one or more optical detectors are disclosed in U.S. Patents 3,496,364; 3,524,067; 4,114,034 and 4,180,704. However, none f these optical tracking devices discloses optical tracking techniques suitable to perform the functions required in a mouse, i.e., they are not "smart" enough to provide multidirectional tracking indicative of direction of movement and the amount of that movement. What may be even more acceptable is an optical cursor control, i.e.,

an optical mouse that detects motion relative to the mouse body and independent f mouse rotation and independent of any inherent coordinate system employed with the mouse for tracking.

According to this invention, a sensor array is disclosed comprising a plurality of sensor cells capable of forming distinguishable bitmap images employing a mutual correspondence scheme relative to neighboring sensor cells. Further, the sensor array may be employed in a cursor control device to provide for cursor movement on a display screen in an interactive display oriented computer system.

The sensor array comprises an array of sensor cells capable of sensing radiation. The cells are connected in a manner to form distingiushable bitmap images through a pattern of correspondence among the cells. Each bitmap image formed comprises a combination of one or more cells indicative of detecting a image pixel within a field of array cells that have been nonindicative of such detection. The pattern of correspondence may be one of inhibition of the operation of other cells in the array or one of indication of operation to other cells in the array.

In one form of the invention, circuit means, implemented in VLSI, e.g., NMOS integrated circuitry, is connected to each of the sensor cells to inhibit the response of at least one adjacent sensor cell in the array when an inhibiting cell has sensed a sufficient quantity of radiation, the pattern of inhibition among the sensor cells being creative of a multitude of bitmap images. Each bitmap image produced comprises responsive sensor cells in the array that have sensed radiation and non-responsive sensor cells in the array which either have not sensed radiation or have been inhibited from responding by one or more of the responsive sensor cells. Thus, the responsive cells create a bitmap image within the metes and bounds of the sensor array.

One way to create a bitmap image within the sensor cell array is to provide a contrasting pattern comprising a plurality of features on a contrasting background. The pattern is illuminated and the radiation is focused from the contrasting pattern onto the sensor array. The contrasting pattern may comprise a plurality of light features on a dark background r dark features on a light background. The features may be, for example, dots, spots or lines.

As employed in a cursor control device or optical mouse, the circuit means includes circuitry and a finite state machine comprising a programmed logic array responsive to changes in the bitmap images and capable of generating coordinate signals to a visual display device corresponding to changes in positional movement of the mouse relative to the contrasting pattern and, correspondingly, represent positional changes in the position of a visual cursor on a display screen of a display oriented computer system.

The invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a system utilizing the sensor array of this invention.

Figure 2 is an enlarged perspective view to explain the relationship of a sensor array relative to a contrasting pattern employed in accordance with this invention.

Figure 3 is an enlarged plan view of a sensor array to explain the theory of sensor cell inhibition.

Figure 4 is an example of neighbor inhibition in a three-by-three array.

Figure 5 is an example of neighbor inhibition in a four-by-four array.

Figure 6 is an enlarged view relating to neighbor inhibition scheme in a linear array.

Figure 7 is a plan view of linear patterns to explain the linear neighbor inhibition possible with the scheme of Figure 6.

Figure 8 relates to the potential inhibition patterns for the neighbor inhibition of Figure 7.

Figure 9 is an enlarged view relating to modified neighbor scheme inhibiti n in a linear array.

Figure 10 is a plan view f linear patterns to explain the linear neighbor inhibition possible with the scheme of Figure 9.

Figure 11 relates to the potential inhibition patterns for the neighbor inhibition of Figure 10.

Figure 12 is an illustration of the number of bitmap images possible for a four-by-four array based upon the extent of inhibition radius.

Figure 13 is a detail of all the 30 possible patterns for the four-by-four sensor array having an inhibition radius of 3.0.

Figure 14 illustrates various positions of a four-by-four sensor array relative to a hexagonal dot contrasting pattern showing examples of possible stable patterns for 3.0 inhibition radius.

Figure 15 illustrates another form of pattern characterization of the four-by-four array having a 3.0 inhibition radius.

Figure 16 is a circuit diagram for a single sensor cell in a sensor array.

Figure 17 is a simple logic diagram for the circuit shown in Figure 16.

Figure 18 is a circuit diagram for two connected sensor cells in a sensor array.

Figure 19 is a simple logic diagram for the circuit shown in Figure 18.

Figure 20 diagramatically illustrates a linear motion detection scheme utilizing a contrasting pattern comprising light features on a dark background.

Figure 21 is a logic diagram for the operation of the detection scheme of Figure 20.

Figure 22 is a diagramatic illustration of a cursor control device or optical mouse comprising this invention utilizing IC chip including the circuitry and logic illustrated in Figures 23 through 30.

Figure 23 is a block diagram illustrating a finite state machine having a programmed logic array to provide an output based upon a comparison between a present and previous bitmap produced by the digital imager.

Figure 24 is a logic diagram illustrating the timing logic and clock signals for the machine of Figure 23.

Figure 25 is a timing diagram illustrating the operation of the logic shown in Figure 24.

Figure 26 is an illustration of tracking relative to a contrasting background by comparing old and new bitmap images.

Figure 27 is a logic diagram for the tracker PLA and counters specifically for implementing cursor control using the finite state machine of Figure 23.

Figure 28 illustrates all the possibilities for sensor cell change between a previous and present bitmap.

Figure 29A illustrates a portion of an old-new bitmap matrix table for explaining tracking movements as interpreted by the logic circuitry of Figure 27.

Figure 29B is a partially filled in table and legends illustrating the moves necessary for tracking bitmap images with the optical mouse.

Figure 30 is a logic diagram for a portion of the circuitry for a cursor control device comprising this invention.

Figure 31A is an example of part of the circuitry in Figure 30, the example being relative to detecting for a positional function, MOVED DOWN RIGHT.

Figure 31B is an example of operation of the circuitry in Figure 31A relative to a cell array in detecting the positional function, MOVED DOWN RIGHT.

Figure 32 is a more detailed logic diagram of the tracker PLA and counter of Figure 27 for X tracking movements, the logic circuitry being identical for Y tracking movements.

Figure 33 is a symbolic logic representation of the conflict resolution circuitry of the tracker (PLA) in Figure 32.

Figure 34 is a symbolic logic representation of the circuitry of the X counter (PLA) in Figure 32.

Figure 35 is a logic diagram for a linear detection scheme similar to Figure 20 except utilizing a contrasting pattern comprising dark features on light background.

Figure 36 is an illustration of additional subsets of bitmap images possible for a four-by-four array and a contrasting pattern comprising dark features on light background based upon given inhibition radii.

Figure 1 represents a generic characterization of this description and may be referenced as a digital image system. The components of the system are represented by the components 10, 12, 14, 16 and 18 in Figure 1. A scene or image 10 is present for detection. The optical scene is received by a detector array, digitized in a preferred manner, and processed to produce a desired signal output. The illuminated optical input scene 10 is detected by the analog sensor array 12, usually with the aid of focusing with an optical lens. The sensor array 12 is responsive to produce a bitmap image. This response undergoes digital image processing by means of logic circuitry, also termed imager, 14. At this point, the bitmap image is connected into an electrical representation of the originally sensed image. Further data processing at 16 produces desired interpretations of these patterns usually in the form of electrical signals that have meaning to and are interpreted by a utilizing device, user system or host 18.

In the framework of this disclosure, the various components 10, 12, 14, 16, 18 are related to the description and figures as follows.

The optical input scene 10 comprising a contrasting pattern is best shown in Figures 2, 14 and 20. The contrasting pattern comprises a plurality of features on a contrasting background. The features may be light representations on a dark background or dark features on a light background. The features comprise geometric shapes, such as a plurality of dots, squares, lines, bars, etc.

The sensor array 12 may comprise a two-dimensional array illustrated in Figure 2 or a linear array illustrated in Figure 20. Each array is made up of a group of sensor cells 20 having the logic attributes as disclosed in Figures 16 and 17.

The digital image processing or imager 14 is best illustrated by the logic circuitry of Figures 18, 19 and 21. The output 15 of the imager 14 is representative of a bitmap, i.e., each sensor cell represents an independent picture element or pixel, which together form the array. A bitmap is produced in the array by some of the cells being responsive to the optical input scene 10 while others are not.

Data processing 16 is best illustrated in Figure 21 and Figures 26 through 33. The utilizing device for the purposes of exemplification of the invention comprises a cursor control device to provide movement for a visual cursor from position to position on the display screen of an interactive display oriented computer system. The cursor control device or optical mouse is illustrated in Figure 22. The manner of operation of the sensor array 12 and imager 14 is a unique feature of this invention and a particular application of the sensor array is its employment as a cursor control device in conjunction with a visual display. The concepts of mutually inhibiting and/or self timed light imaging are not limited to cursor control devices. Other applications may be, for example, pattern or character recognition, optical alignment, edge detectors, light controlled oscillators, etc.

Figure 2 illustrates one embodiment of components 10 and 12. The sensor array 12 comprises a two-dimensional array of sensor cells 20, in this case being a four-by-four array. The scene 10 comprises a contrasting pattern 22 having features 24 on a contrasting background 26. The features 24 are larger in area than the sensor cells 20. The sensor array 12 is analogous to a fly's eye and "looks" at the pattern 22. Some of the cells will be responsive to light from the pattern 22, for example, radiation provided from source 17 and reflected from the features 24, these features being light features on a dark background.

Also, the light may be projected through the pattern 22 rather than reflected from the pattern. Radiation source 21 may be used in lieu of source 17 for this purpose. Under these conditions, the features 24 may be translucent or transparent while the background 26 is paque.

The pattern 22 is depicted as planar but it should be realized that this pattern may be on

a contoured surface. For example, pattern 22 may be n the exterior surface of a sphere with the sensor array 12 positioned centrally within or externally adjacent to the sphere surface with relative movement provided between the sphere and array for tracking.

An important feature of the invention is the manner of digital bitmap creation by the imager 14 and sensor array 12. The circuitry involved produces digital image snapshots of the contrasting pattern 22 employing self timed circuit techniques and mutually inhibiting sensor cells or neighbor cell inhibition. This concept is explained relative to Figures 3-5 for two-dimensional arrays. A form of inhibition is implemented between sensor cells 20 in a manner that the output of some cells have reached a different logic state due to response to light detected while others are held to the original logic state either because they have been inhibited from detecting light by a nearby responsive cell or because they have detected insufficient radiation. Once each cell has either detected light or has been inhibited by another responsive cell, the image is stable. All cells form a stable bitmap image until the digital logic is reset to commence the formation of a new snapshot. The digital imager 14 with its self timed logic can establish stable patterns, latch the patterns, reset and start over again at a rate roughly proportional to and independent of the light level. Thus, a nice feature of the imager is that it is substantially light level independent.

As will be explained in greater detail later, the number of possible bitmap images depends on the degree of neighbor inhibition. Also, the sensibility and practicality for pattern use depends, to some extent, on the degree of inhibition. In Figure 3, the degree of inhibition is represented by various radial extensions, R_1 to R_n from a sensor cell 20' that has been responsive to light. The greater the extent of inhibition means a decrease in the number of sensor cells 20 that will be responsive to light in any given image or snapshot.

Possible sets of stable output patterns due to neighbor inhibition is illustrated in Figures 4 and 5. In Figure 4, a three-by-three sensor array is shown with the degree of inhibition being immediate neighbor cells. This represents the smallest degree of inhibition. This is represented by Figure 4A where the "1" level represents a responsive cell in the array. The cells at the "0" level are, therefore, inhibited. This leaves the cells marked "x" in the array, which have the possibility of being either "1" r "0" prior to array reset. Figures 4B-4I represent all possible stable patterns for this particular degree f inhibition.

On the other end of the spectrum, the largest degree of inhibition would be that each

sensor cell in the three-by-three sensor array of Figure 4 is connected to every ther sensor cell in the array so that upon the response of one cell in the array, every other cell is inhibited from response. In the three-by-three array, this provides the possibility of nine bitmap images.

By making the array larger, the number of possible patterns becomes larger. In Figure 5, a four-by-four sensor array is shown with the degree of inhibition being again immediate neighbor cells. This is represented by Figure 5A where the "1" level represents a responsive cell in the array. The cells at the "0" level are, therefore, inhibited. This leaves the "x" marked cells with the possibility of being either "1" or "0". This results in the possibility of creating seventy-nine stable bitmap images, three of which are illustrated in Figures 5B-5D. This set of bitmap images has an interesting property of having a "1" level in each quadrant of the array.

Figures 6-11 illustrate linear arrays for linear tracking and employing a near neighbor inhibition concept. Assume a linear array of four sensor cells. Various positions of the array relative to a contrasting pattern 22 is represented by the four groups of dots, A, B, C and D in Figure 6. The four sensors would be alternately coupled to form pairs so that one cell would not inhibit its immediate neighbor but rather the next succeeding cell. This alternate coupled pair of sensor cells is illustrated by the arrows in Figure 7. With this scheme, four patterns are possible as illustrated by Figures 7A-7D. The arrows extend from responsive cells ("1" level) and indicate inhibition ("0" level) of alternate cells. The creation of inhibition using a contrasting pattern 22 is illustrated in Figure 6. The pattern 22 consists of a linear grid comprising alternating light strips 28 and dark strips 30. Sensor cells that are responsive to light reflected from strips 28 are shown as dark spots in groups A-D. The patterns produced by groups A-D in Figure 6 match with those of Figure 7, the latter figure illustrating the alternate neighbor inhibition.

If the strip widths of the pattern 22 are equal to about twice the sensor spacing in the array, these patterns correspond in a readily determinable manner to positions of the strips relative to the sensors.

The possibilities in the development of any one f these patterns after one cell has been responsive is disc sed in Figure 8. The possibilities are indicated by cells marked "x" where "x" will become either "0" or "1", depending on cell response.

The case of the linear array of Figures 9-11 is different from Figures 6-8 in that the contrasting pattern 22 comprises light strips 28' and dark strips 30' having different strip widths. The light strips 28' are of narrower width than the dark strips 30' by about one-third. With the light strip spacing being about equal to about three sensor cell widths along the linear array, three stable patterns are possible with a neighbor inhibition the same as the previous case of Figures 6-8. The three patterns are shown in Figure 10 with the neighbor and alternate neighbor inhibition illustrated by the arrows. The possibilities in the development of any one of these patterns after one cell has been responsive is disclosed in Figure 11. The possibilities are indicated by cells marked "x", where "x" will become either "0" or "1", depending on cell response. As compared to Figure 8, the possibilities have been narrowed due to the change in the widths of the light and dark strips 28' and 30'.

The alternate neighbor inhibition concept used in these linear arrays can also be readily applied to two-dimensional arrays.

A simple digital finite state machine on the same semiconductor chip as the linear sensor array can be created for the purpose of comparing the current bitmap image with the previous bitmap image and produce output signals indicative of the positional functions, such as, "moved left", "moved right" or "stayed". Such an uniaxial or unidimensional motion sensor will be discussed in further detail in connection with Figures 20 and 21.

A greater challenge is presented for multidirectional sensing utilizing a two-dimensional array which is tolerant of rotation of the sensor array relative to the contrasting pattern. Before proceeding with discussions relative to logic circuitry for the sensor array 12 and the imager 14 for linear or two-dimensional arrays, further explanation of patterns of inhibition relative to two-dimensional arrays should be first given.

Figure 12 illustrates the total number of images possible for four-by-four sensor arrays for different radii of inhibition, measured in units. The number of stable bitmap images are pictorially illustrated followed by how many of those "types" of images are possible. The responsive sensor cells in the array are indicated as dark cells (■). By "types" it is meant mirror images or rotations of images in the same array f r a given image. "Inhibition neighborhoods" in Figure 12 represents pictorially the extent or degree of inhibition. The dark cells (■) represents the responsive cell, the inhibited cells are shown

nonexistent as background, while cells that may still be responsive because they are outside the radius of inhibition of the responsive cell, are indicated by plus signs (+). According to the degree of inhibition, neighboring sensor cells in an array are coupled to sensor cells responsive to light and are inhibited from being responsive themselves, i. e., forced to stay at their original original binary level, i.e., "0".

Out of the different groups of images for given inhibition radii, one may select the group most suitable for a particular application. For applications relative to cursor devices, the image group having a radius of 3.0 is chosen for illustration. As indicated in Figure 12, this group provides a set of 30 stable images, which are all illustrated in Figure 13. These images comprise one or two responsive cells in the array per image. This particular inhibited sensor array may be employed in association with a contrasting pattern 22 comprising a hexagonal array of light or white dots 24 on a dark or black background 26, illustrated in Figure 14. Preferably, the white dot spacing is slightly more than the inhibition radial distance. For example, in the 3.0 inhibition radius sensor array, the dot spacing in the contrasting pattern 22 may be about 3.2, which is about the average distance between responsive cells in images formed by such an array.

The sensor array with a 3.0 radius of inhibition and the rule of thumb dot spacing provides for a set of detectable images that make it simpler to translate them into image tracking. A unique characterization of these images is evident from an examination of the images in Figure 13 with the aid of Figure 15. The 30 images fall into two classes. The image is either a single responsive cell that falls in the central quad 32 of cells or it is a pair of responsive cells that fall in linear edge quads 34 on opposite sides of the array but never along the same edge of the array or sharing an edge of the array. In any case, there is always a feature or dot to track, as depicted in Figure 14, upon movement of the sensor array 12 relative to the contrasting pattern 22.

The simplest form of a cell 20 within an array 12 is shown in Figures 16 and 17 while the simplest form of a sensor array imager with mutual inhibition is illustrated in Figures 18 and 19. NMOS integrated circuit technology was used in the actual implementation of the invention but other integrated circuit technologies (PMOS, CMOS or bipolar) may be employed. In NMOS, when light strikes the circuit areas of the chip, photons are converted into hole-electron pairs with some reasonable quantum efficiency. The holes are attracted to the p-type silicon substrate, the most negative voltage region, while electrons are attracted into n-type diffused regions, e.g., conductors, and channel regions, particularly those at higher potential.

Referring to Figure 16, each sensor array cell 20 comprises a dynamic node 36. Node 36 is a circuit node which is isolated by low impedance transistor 38 and normally is capable of holding its voltage level for long periods of time due to its capacitance to ground 44. This capacitance is represented at 40. The photo-diode 42 represents the light detective properties and is connected to ground or a negative bias 44. When RESET is high or "1", transistor 38 is on and VDD charges the dynamic node 36. When RESET is low or "0", then transistor 38 is off and the charged node 36 is isolated from VDD. Light is detected by the cell 20 due to the sensitivity of photo-diode 42 causing it to collect negative charge. As a result, there is a decrease of voltage at node 36. The voltage at node 36 continues to decrease as the diode 42 continues to be responsive to the presence of light.

The declining voltage at node 36 may be monitored by employing an inverter circuit 45 represented by transistors 46 and 48 to sense the voltage of the node 36 and communicate it as an output 50. The operation of this inverter circuit is conventional and is disclosed and discussed in the book, "Introduction to VLSI systems" by Carver Mead and Lynn Conway and published by Addison-Wesley Publishing Company, Chapter 1, pages 5-10. The inverter provides the complement. For example, upon each RESET and charging of the dynamic node 36, the voltage output 50 will start low and then rise toward a higher voltage as the dynamic node 36 goes low due to the detection of light and depletion of positive charge across the diode 42.

Figure 17 is schematic diagram of cell 20 which comprises a light detector reset by an input and coupled to an inverter to provide a high or "1" output when the detector output goes low or "0", until RESET.

The imager 14, therefore, may be characterized as an array of cell subcircuits each with a dynamic node capable of "watching" declining voltages and producing pixels, together forming partial bitmap images based upon inhibiting continued operation of other neighboring cell subcircuits. The simplest imager form is shown in Figure 18. The intercell connection is only illustrated for two cells for purposes of simplicity. The schematic diagram for the circuitry of Figure 18 is illustrated in Figure 19.

The two cell imager 14 comprises cells 20, a done detect circuit 62 and a ready detect circuit 64. Each cell 20 has a NOR gate 60 (Figure 19) at its output which has its utput cross coupled as an input to the NOR gate 60 of the other cell. The outputs of the NOR

gates 60 are connected to an OR gate 62 whose logic threshold is higher than normal. The outputs of NOR gates 60 are also connected to NOR gate 64 which has a lower threshold than normal. The two cell imager 14 compares the light level at two cell nodes 36 and provides an indication when it has made a decision. Either PIXEL LIGHT -1 or PIXEL LIGHT -2 output will be high when the output of OR gate 62 is high ("1"), meaning that the cells have completed their light sensing function and the signal DONE is high or "1".

OR gate 62 consists of a NOR gate comprising two transistors 61 and an inverter comprising pull down transistor 63. The output of the transistors 61 is the signal CELL DONE.

The symbol (*) on the NOR gate 64 means that this gate is a low threshold NOR gate, i.e., the threshold of operation is below normal so that its output will not indicate true until both inputs to the gate are definitely low, which indicates that precharge of the senor nodes 36 has been successfully accomplished. Thus, a READY signal that is high or "1" indicates that both PIXEL LIGHT-1 and PIXEL LIGHT-2 are low or "0", meaning that RESET has been accomplished. The symbol (#) on the OR gate 62 means that this gate is a high threshold OR gate, i.e., its output is not true until either input is definitely high so as to ensure that intermediate and metastable states have passed. Thus, a DONE signal indicates that either PIXEL LIGHT-1 or PIXEL LIGHT-2 has definitely gone high or "1".

Looking at the operation of the cross-coupled NOR gates 60 from a binary pattern point of view, the initial reset pattern of the NOR gates 60 is 00, since the outputs are low because the initially high dynamic nodes 36 are high or "1". The final pattern after intermediate and metastable states can only be either 01 or 10, since the NOR gate output pattern, 00, will decay with time and the pattern, 11, is not a possible output from the cross-coupled NOR gates.

The concept illustrated by the two cell imager 14 is the use of cross-coupled transistors to convert the image sensing inverters of the cells to NOR gates 60. Any pair of cells in the sensor array 20 may be chosen to be connected by these mutual inhibition sub-circuits 20. For example, each cell may be connected with its eight neighbor cells in a square grid, resulting in nine input NOR gates 60.

In any mutually inhibiting sensor array and imager, the cells 20 "race" to see who will finish first within an inhibiting neighborhood by obtaining enough light and then inhibiting other cells in the neighborhood from being effective. This functioning is described in connection with a linear sensor array and logic disclosed in Figures 20 and 21. The linear array is initially chosen for illustration because it is simpler to understand as compared to a two-dimensional array, which will be described later. However, the principle of operation is fundamentally the same.

In Figure 20, the imager comprises the IC sensor chip 70 having a linear array of cells 20 coupled to circuit logic 72. Logic 72 for the most part is illustrated in Figure 21. The chip 70 in combination with the contrasting pattern 22 of alternate light and dark strips 28 and 30 represents a complete digital image system from component 10 to component 16 in Figure 1 to provide a signal output 19 to a user system 18. The pattern 22 in Figure 20 is the scene 10. The sensor array 12 is represented by the linear array of cells 20. The circuit of Figure 21 represents the cell array as well as both the imager 14 to the point output of AND gate 80 and signals DONE and SPOT DETECTED, and data processing 16 to the point of output of the 4-state counter 92 and the quadrature signals.

In Figure 20, imaging optics 74 focuses the light image from pattern 22 onto the linear array 12. Relative movement between the contrasting pattern 22 and chip 70, indicated by arrow 76, will be productive of various linear bit patterns, which, upon sequential comparison, can be indicative of the positional functions, MOVED DOWN or MOVED UP. The absence of either of these signals means no motion detected or STAYED.

With reference to the schematic circuitry of Figure 21, four binary logic variables are involved: SENSOR NODE, PIXEL LIGHT, SPOT DETECTED and CELL DONE. Starting the cycle of operation is accomplished by raising RESET to high, resetting SENSOR NODE equal to "1" which, in turn sets PIXEL LIGHT, SPOT DETECTED and CELL DONE to "0" in each cell 20. Once reset of the nodes 36 is accomplished, READY, the output of low threshold NOR gate 64, will go high and cause the timing logic 82 to set RESET low. At this point, array 12 is set to detect radiation received from pattern 22.

Upon operation of the sensor array 12 and logic 70, the following events occur. SENSOR NODE will slowly discharge from its reset high value from a 1 to 0 as light is detected by a responsive cell or cells. PIXEL LIGHT is the result of the low threshold NOR gate

60 function, the gate 60 having several inputs, one connected to the dynamic node 36 of its respective cell to receive SENSOR NODE and the other inputs being the cross coupled outputs from some of the other NOR gates 60 in the neighborhood. The number of inputs is dependent on the degree of inhibition. In the particular case here, the inhibition pattern is that of Figure 11. The inhibition network among the outputs and inputs to NOR gates 60 is defined by choosing an inhibition neighborhood for each cell. Generally, neighborhoods are chosen to be symmetrical across the array, such that, since PIXEL LIGHT -1 inhibits NOR gate 60-2, then PIXEL LIGHT -2 will inhibit NOR gate 60-1. In many cases, the inhibition neighborhood of some cells may be all other cells in the sensor array.

The high or "1" produced at a NOR gate 60 output, PIXEL LIGHT, is connected to the input of the high threshold buffers 78 with their output designating a detected cell image, SPOT DETECTED. The output of the buffers 78 are connected as inputs to each of the OR gates 79-1 to 79-4. In order to signify that all detection functioning from each of the cells is complete, each of the four OR gates 62 must produce a done-detect signal CELL DONE. The CELL DONE signals from gates 79-2 and 79-3 are redundant and not necessary but may be just as well implemented for the convenience of circuit layout.

The inhibition NOR gate 60 output, PIXEL LIGHT, itself is not used for the final done-detection function. Rather a buffered version of that signal is used for the done-detection function, after passing a high threshold buffer 78 comprising a pair of inverters. This output signal is designated SPOT DETECTED and is indicative of the pixel condition of a cell. This is a simple way of preventing false done-detection during a metastable condition. The buffered signal is not used for inhibition, since that would make it participate in the metastable conditions, and because the extra delay included could cause oscillatory metastable states.

The outputs of each of the four OR gates 79-1 to 79-4 are connected as inputs to AND gate 80. AND gate 80 provides an output signal, DONE, to the timing logic 82.

Timing logic 82 provides two clock signals, PHI-SHORT and PHI-LONG. Details of the timing logic will be discussed later relative to Figure 24. Timing logic 82 also provides the signal RESET, as previously indicated.

Low threshold NOR gate 64 has four inputs connected to receive all SENSOR NODE

signals from the cells 20 and produces at its output the signal, READY, to timing logic 82, which is high or "1" when all of its inputs, the PIXEL LIGHT signals, are all set low or "0", meaning that all points SENSOR NODE are high.

The SPOT DETECTED signal outputs are also connected to a 4-bit parallel register 84. Register 84 is conventional and is shown in greater detail in Figure 30. Also, more information relative to registers can be found in Chapter 3 of the book, "Introduction to VLSI Systems", supra. The output of register 84 always represents the previous bitmap image represented by signals, OLD SPOT, while the input to register 84 represents the just detected bitmap image represented by the signals, SPOT DETECTED. Register 84 performs the function of a latch. Operation of register 84 is accomplished by the clock signals PHI-SHORT and PHI-LONG. Clock PHI-LONG places the input into register 84 and clock PHI-SHORT places the input at the output of register 84. The clock signals PHI-SHORT and PHI-LONG are also connected to a 4-state counter 92.

The SPOT DETECTED and OLD SPOT signals are connected to down comparator 86 and up comparator 89. Comparator 86 comprises three AND gates 87 having inputs respectively connected to the signal lines SPOT DETECTED -2 and OLD SPOT -1; SPOT DETECTED -3 and OLD SPOT -2 and SPOT DETECTED -4 and OLD SPOT -3. The outputs of AND gates 87 are connected as inputs to OR gate 88. The output of OR gate 88 is a MOVED DOWN signal connected to the D input of counter 92. Comparator 89 comprises three AND gates 90 having inputs respectively connected to the signal lines SPOT DETECTED -1 and OLD SPOT -2; SPOT DETECTED -2 and OLD SPOT -3 and SPOT DETECTED -3 and OLD SPOT -4. The outputs of AND gates 90 are connected as inputs to OR gate 91, the output of which is a MOVED UP signal connected to the U input of counter 92. The absence of a signal on either input D and U during the appropriate clock cycle means STAYED.

The outputs of counter 92 are COUNT A and COUNT B and represent a quadrature signal output to a user system or device. Quadrature signalling relative to counter 92 is a state of the art technique and has been used with conventional electromechanical mice for many years. The 2 bit counter 92 is used to convert the MOVE UP and MOVE DOWN signals into quadrature signal representations convenient for asynchronous sampling by the user system 18 to which they are connected. The signal STAYED is, in essence, a NOR gate function when the outputs of OR gates 88 and 91 are low or "0", indicating no MOVE UP or MOVE DOWN.

It is a matter of design to provide desired feature spacing in contrasting patterns, the degree of array inhibition, the number of cells in an array, etc., depending on what is desired relative to a particular linear motion situation and intended solution. The bigger challenge comes with two-dimensional detection and universal movement of the detecting array relative to a contrasting pattern. Such a challenge is an extension of the unidimensional tracking device disclosed in Figures 20 and 21 and will now be discussed.

Figure 22 is a schematic side elevation of a cursor control device or optical mouse 100 comprising this invention. Structurally, the mouse 100 looks like conventional electromechanical mice. However, internal mechanical moving parts are replaced by the VLSI chip 102, mirror 104, lens 105 and light source 106. Housing 108 supports the PC board 110 upon which is mounted the structure 112 to support the chip 102. Chip includes the integrated circuitry for the sensor array 12, image processing 14 and data processing 16, including other appropriate circuitry, such as timing circuitry. Quadrature signal output to the user system 18 is along cable 113. Function switches may be provided in the top of housing 108, each comprising a button 116 operative of a microswitch 114. Finger pressure on button 116 will depress stem 115 of microswitch 114. Microswitch 114 is supported on and electrically connected to PC board 110. The depression of button 116 will activate switch 114 and provide a signal to user system 18 to initiate a desired system function.

In use, the mouse 100 is moved over the work surface that includes the contrasting pattern 22. The light source 106 in mouse 100 illuminates a portion of pattern 22 as the mouse is moved over the surface of the pattern. The illuminated light features of the pattern 22 are focused by lens 105 on the surface of the IC chip 102 which includes sensor array 12.

The sensor array 12 and imager 14 having been discussed in detail, reference is now made to the data processing 16 and bitmap interpretation to provide a cursor tracking system useful for cursor control on display screens. This is accomplished by a finite state machine illustrated in Figure 23. For discussion as to what is meant by a finite state machine, reference is again made to the book, "Introduction to VLSI Systems", supra, Chapter 3, pages 82-88. The data processing 16 comprises a programmed logic array (PLA) 120 which includes tracking logic and counters to provide an output indicative f the amount and direction f movement of the optical mouse 100 relative to a contrasting pattern 22. The PLA 120 is copuled to the timing logic 126 to provide two clock inputs,

bitmap image input 15 from imager 14 and quadrature signal output 19 to the utilizing device 18, in this case an interactive display oriented computer system. Figure 24 shows details of the timing logic 126, which provides two phase nonoverlapping clock signals, PHI-SHORT and PHI-LONG.

In general, the PLA receives a stable bitmap image along input 15 and compares this with its current state, which most likely is the previous image input and provides an output indicating the direction of movement of the mouse 100 relative to the pattern 22 based on the current state and new input. The output signal 19 represents a new state that can be understood by the user system 18 and indicative of relative motion of the imager/mouse.

The timing logic 82 and 126 are essentially the same. Logic 126 permits the PLA 120 to be self timed in performing the tracking function as well as control the tracking logic that generates two pairs of quadrature signals on output 19. The timing logic 126 generates the two phase clock signals to run the PLA 120 such that each cycle is synchronized to the reset-done cycle of the imager 14. The same clock signals run the counters controlled by the PLA to generate quadrature signals which can be converted to TTL compatible levels for communication off chip.

The timing logic 126 includes an input of a stable image from the imager 14 via AND gate 181 for the signal DONE to the input of the inverter 128. The output of inverter 128 is connected to NOR gate 130. The output of NOR gate 130 is cross-coupled to be an input of NOR gate 132. The output of NOR gate 130 is also connected as an input to NOR gate 134. The signal output from NOR gate 130 to inputs of NOR gates 132 and 134 is termed, STOP. The output of NOR gate 134 is the signal PHI-LONG and is an input to PLA 120 as well as being cross-coupled as an input to both NOR gates 132 and 136. The output of NOR gate 132 is the signal RESET and is connected to the reset terminal of the transistors 38 in the sensor array cell 20 in the imager 14.

The other input of NOR gate 136 is an output from imager 14, to wit, signal READY from the low threshold NOR gate 64 in the imager 14. The output of NOR gate 136 is the clock signal PHI-SHORT and is an input to PLA 120 as well as cross coupled as an input to both NOR gates 130 and 134.

The operation of the timing logic 126 relative to the imager 14 and the PLA 120 is

explained with reference to the timing waveform diagram of Figure 25. The clock signals are generated through a self-timed handshake with the imager 14. The digital logic of PLA 120 is sufficiently fast to keep up with the operation of the imager 14. The designation for the clock signals are chosen to indicate that PHI-LONG is of unbounded length compared to PHI-SHORT. The phase of PHI-LONG is during the "watching" period within which period bitmap images are formed. The phase of PHI-SHORT is during "cycling" period of the logic. PHI-LONG is also used as a quasi-static feedback to keep the PLA logic enabled and insensitive to any light on the chip surface while waiting for the report of results from the imager 14. The steps of operation of the timing logic 126 are as follows.

The operation starts with the initial scene sensing state just after RESET goes to "0". A high or "1" READY signal from imager 14 means that all PIXEL LIGHT signal outputs are at a low or "0". The DONE signal input at inverter 128 is at low or "0", meaning that there is presently no stable bitmap image. The output PHI-LONG at NOR gate 134 is high or "1" because, initially, it is at this binary level during the longer watching clock phase. Because of the cross coupling in the timing logic 126, this means that the output, PHI-SHORT, is low or "0". The output STOP at NOR gate 130 is low or "0" because a bitmap image is not yet complete, i.e. DONE is low or "0".

Reference now should be made to Figure 25 while following along in reference to Figures 16-19, 21 and 24. After some light has been received on the sensor array 12, some PIXEL LIGHT outputs will start to rise toward high or "1". Note in Figure 25 the decrease in SENSOR NODE voltage value and an increase in PIXEL LIGHT voltage value. At some time before the bitmap picture and cell operation is complete, READY will go low or "0". The exact time is not important. This time is illustrated at 140 in Figure 25. Note that the PIXEL LIGHT outputs are still rising.

When enough light has been received and detected, one or more SPOT DETECTED outputs will go high or "1". This is indicated at 141 in Figure 25. The bitmap image has become stable pattern at this point in time. Next, a series of events will occur, leading to the short clock phase and cycling. Each cell reports CELL DONE to AND gate 181 and AND gate 181 reports DONE r "1" to inverter 128 (142 - Figure 25). The output of inverter is the complement, "0", to the input of NOR gate 130. The other input to gate 130, is already PHI-SHORT equal "0". As a result, the output, STOP, of gate 130 goes high or or "1" (143 - Figure 25). The inputs to NOR gate 134 being now at "0" and "1",

(previously "0" and "0"), the utput PHI-LONG, of gate 134 goes low r "0" (144 - Figure 25). With both PHI-LONG and READY at "0" the output of NOR gate 136 will go high or PHI-SHORT equal to "1" (145 - Figure 25).

With PHI-SHORT at "1", the inputs to NOR gate 130 are "0" and "1". The output, STOP, of gate 130 will now go low or "0" (146 - Figure 25). Since PHI-LONG is "0" and STOP is "0" (inputs to NOR gate 132), the output, RESET goes high or "1" (147 - Figure 25). RESET at high will turn on transistors 38 in the imager 14, permitting the charging of dynamic nodes 36 (148 - Figure 25), i.e., SENSOR NODE equal "1". Because of this, the pulldown transistors 46 will eventually turn on and pull PIXEL LIGHT to ground and the output PIXEL LIGHT will go low or "0" (149 - Figure 25). As a result, CELL DONE and DONE will go low or "0" (150 - Figure 25).

At about the same time, the output READY will go high or "1" since all outputs, SENSOR NODE equal "0" (151 - Figure 25), which is the functioning of NOR gate 64. At this time, READY input to NOR gate 136 will be high or "1" and the PHI-LONG input will be low or "0". As a result, the output, PHI-SHORT, of gate 136 will go low or "0" (152 - Figure 25). With both the outputs STOP and PHI-SHORT equal "0", gate 134 will go high or "1" (153 - Figure 25) and with STOP and PHI-LONG respectively at "0" and "1", the output RESET of gate 132 will go low or "0" (154 - Figure 25). Thus, the long and short clock phases of one cycle is completed with the value for initial state conditions being at the binary values as originally stated above.

Reference is now made to tracking aspects, i.e., the manner of interpretation of a positional move relative to a detected change from one bitmap image to the next.

As previously indicated, for a two-dimensional array, the degree of inhibition chosen was radius equal 3.0, providing 30 stable patterns as disclosed in Figure 13. A matrix of these stable patterns can be formed so that 30 patterns may set up along a horizontal coordinate and the same 30 patterns set up along a vertical axis. One set may be termed, "old pattern" and the other set termed "new pattern". The resulting matrix will provide up to 900 possibilities of interpretation when translating from an old pattern to a new pattern. However, not all 900 possibilities are necessary for feature tracking with the optical mouse 100. A small portion of the matrix table is shown in Figure 29A and will be referred to in the discussion below. Figure 29B shows a partially filled in matrix table with all 900 possibilities represented. The legend at the bottom of the table is used to interpret the markings in the table.

The comparison functions of bitmap images can be performed in logic circuitry of data processing 16 for a two-dimensional, four-by-four sensor array. The decision as to what happens relative to each cell 20 in the array 12 can be done locally. Each cell, for example, can save its old pixel value ("0" or "1") in a local register. During each cycle, a comparison is made between its new value and its old and also with the value of all its neighbors. Each cell reports out one of eleven possible results which can be characterized with reference to Figure 28. Cell 20 can report, for example, that its previous pixel value of "1" has "moved" to one of its eight adjacent neighbor cells (up, up right, right, down right, down, down left, left or up left), or it stayed here, or it "vanished" (most likely because it became inhibited) or that it didn't have a pixel "1" to track in the first place. With all the cells reporting this information to the PLA 120, a logic decision can be made as to what must be reported, while any contradictions must be filtered out.

The eleven possibilities result in nine of them requiring conflict resolution, which are the eight neighbor moves and the no move (stayed here) of Figure 28. The other two (no "1" present or no "1" to track) need not be reported. These nine inputs are identified as inputs to a tracker PLA 160, shown in Figure 27. The purpose of PLA 160 is to produce counter control signals for X counter 162 and Y counter 164. PLA 160 has eight outputs relative to conflict resolution, three relating to X coordinate values of X UP, X HALF and X FULL, three relating to Y coordinate values of Y RIGHT, Y HALF and Y FULL, ANY GOOD and JUMP. ANY GOOD and JUMP are diagnostic counter control signals and do not relate to the tracking scheme. The eight state X and Y counters 162 and 164 receive these outputs as inputs X RIGHT, X HALF and X FULL and Y RIGHT, Y HALF and Y FULL, respectively. Each of these counters provide a pair of output signals XA and XB; YA and YB for the user system 18. Additional outputs XL and YL from these counters represent half cycle signals. In addition, all of these output signals, representative of current states, are fed back to the input of the counters 162 and 164.

A portion of the old-new bitmap image comparison matrix is shown in Figure 29A. The embodiments shown clearly demonstrate the manner of determining the positional functions of Figure 28. For example, if the previous image is "old" pattern A in Figure 29A and the next pattern is "new" pattern I, the final report would be that the Pixel "1" in cell 20-1 in "old" pattern A moved to a neighbor below, i.e., cell 20-2, as sh wn in "new" pattern I. This is interpreted by PLA 120 as DOWN Y. Another comparison is "old" pattern E to "new" pattern I. Note that the pixel "1" of cell 20-3 in "old" pattern

E has moved to cell position 20-2 in "new" pattern I. Note further that the pixel "1" in cell 20-4 of "old" pattern E has "moved off" of the array. Thus, the resulting interpretation is a move in the positive X direction or UP X. Again, a change from "old" pattern D to "new" pattern II shows that pixel "1" in cell 20-5 in the older image has ended up at cell 20-6 in the new image. Also, a new pixel "1" has appeared within the framework of the array at cell 20-7 in the new image. Thus, these differences can be logically determined as a step movement in both the plus X and minus Y directions or UP X, DOWN Y.

The old-new matrix table may be also used to determine half steps. An example of this is shown in Figure 26. Note that in the comparison between old and new bitmap images that there are two "1" pixels involved. The old image can be identified as pattern number 23 in Figure 13 and the new pattern can be identified as pattern number 9. One pixel has moved down one cell position in the array and the other pixel has moved right one cell position in the array. The two pixel moves, MOVED DOWN and MOVED RIGHT, are interpreted as a half step DOWN RIGHT.

As a further example of half steps, reference is again made to Figure 29A. Note the comparison of "old" pattern E with "new" pattern III. The pixel "1" in cell 20-3 has moved up to cell 20-7 and the pixel "1" in cell 20-4 has moved left to cell 20-8. The two pixel moves, MOVED UP and MOVED LEFT, are interpreted as UP HALF Y and UP HALF X or a half step UP LEFT.

The question marks (?) in the matrix of Figures 29A and 29B indicate no logical correlation between patterns relative to tracking the changes in the positions of pixels "1" in the array from one such pattern to another. The Jumps (J) are pixel movements from one position to another extraneous cell position in the array. They are all treated as contradictions.

As illustrated by the matrix table of pattern tracking in Figure 29B, the pattern matching scheme can be extended to the number of interpretations necessary for tracking the features in the contracting pattern. For the four-by-four array and an inhibition radius of 3.0, thirty pattern matches is all that it is necessary for the matrix and the positional functions identified in Figure 28 out of a possibility of 900 such matches (30 × 30 patterns).

While the particular tracking scheme is demonstrated by Figure 29B for actual tracking of features in a contrasting pattern that is characterized by tracking a feature with the sensor array and logically determining which direction the feature has moved relative to the array, it should be readily understood that pattern comparison logic can be designed for any conceivable old-new pattern matrix table. For example, comparisons need not be based on tracking pixels from one cell to an immediately adjacent or diagonal cell. Tracking could be based upon pixels jumping to predetermined cells in the array and indicative of some function to be performed. An example of this would be an image recognition scheme indicative of some functional message to the user system.

A specific example of the stable pattern detect logic for a two-dimensional array is shown in Figure 30. In order to simplify the explanation and understanding of this logic, the logic circuitry is shown for only one cell, this logic being identical for each of the other 15 cells in the array. The logic circuitry is also shown connected to the sensor array cell 20 and imager 14, previously discussed. Cell 20 is the same except for high impedance transistor 47 connected between node 36 and ground 44 and having its gate connected to the output of NOR gate 60. Transistor 47 is optional. Its function is to accelerate the decison making of the cell by discharging the dynamic node 36 to ground.

The reporting function for any particular cell relative to other cells in the array would be the 9 characterizations shown in Figure 28. The logic circuitryshown has many of the attributes of the circuitry shown in Figures 19 and 21 but is more complex due to the presence of a two-dimensional array.

As shown in Figure 30, the NOR gate 60 will have several cross-coupled inputs from the same NOR gates of other cells 20 in the array 12. The number of such inputs 170 to NOR gate 60 is dependent on the degree of inhibition chosen. Thus, these inputs are PIXEL LIGHT from NOR gates 60 from other cells in the inhibition neighborhood. By the same token, the PIXEL LIGHT output of NOR gate 60 for cell shown in Figure 30 is connected to other cells in the inhibition neighboorhood. The PIXEL LIGHT of all array cell NOR gates 60 are connected as inputs 172 to NOR gate 64, the output of which is the READY signal to the timing logic 126.

The utput 172 of NOR gate 60 is PIXEL LIGHT and is an input to inverter 174 and an AND gate 176A-1, which is one gate of a logic gate pack termed AND-OR (AO) gate 175. The inverted output from inverter 174 is connected to the input of inverter 178

which provides an inverted output SPOT DETECTED. These inverters act as a buffer. The signal level of SPOT DETECTED is the same as that at the output of NOR gate 60. The SPOT DETECTED output is an input to OR gate 179, which also has inputs from other cells in the inhibition neighboorhood. Gate 179 is functionally the same as a gate 79 in Figure 21. The output of gate 179 is CELL DONE and one of the several inputs to AND gate 181, the output of which is signal DONE to the timing logic 126. Gate 181 is functionally the same as gate 80 in Figure 21.

PIXEL LIGHT is the immediate pixel image result of the cell while OLD SPOT is the previous done-detect result of the cell. PIXEL LIGHT is always present as an input to AND gates 176A-1 to 176I-1 of AO gates 175. AO gates 175 comprise groups of AND gates 176A-I, nine gates in each group, with the outputs of the nine AND gates of each group connected as inputs to a respective OR gate 192-1 to 192-9.

OLD SPOT is the other input on line 191 to each of the AND gates 176A-1 to 176I-1. OLD SPOT is an output of a bit register comprising pass transistors 180, 182 and 184 and inverters 186, 188 and 190. This bit register logic is the same as that for the four bit register 84 in Figure 21. The register is, in essence, an master or input latch coupled to a slave or output latch. PHI-LONG operates the input latch while PHI-SHORT operates the output latch. When PHI-LONG is high, the output latch remembers its old input and the input latch is transparent. When PHI-LONG is low and PHI-SHORT is high, then the value at the input latch is transferred to the output latch.

From an examination of this circuitry and the timing diagram of Figure 25, it can be seen that a "present" pixel, i.e., PIXEL LIGHT, is presented as an input to inverter 186 during the watching portion of the cycle, PHI-LONG placing transistor 180 in its "on" state. However, when PHI-LONG goes low at time 144, PHI-SHORT goes high at time 145, transistor 182 is on and inputs to inverter 188. The double inversion PIXEL LIGHT provided by inverter 188 and 190 acts as a quasi-static half register or output latch with an output on line 191 that will represent OLD SPOT during the next cycle in the watching phase of PHI-LONG and the establishment of a new PIXEL LIGHT.

The output f each AND gate 176 represents the condition f each of the nine characterizations in Figure 28 relative to the particular cell 20 under examination. The output of the OR gates 192 represents the characterisations of figure 28 relative to all cells in the array.

Each of the group of AND gates 176A-n to 176H-n receives the signal PIXEL LIGHT from a designated neighbor cell, as indicated in Figure 30. The other AND gates 176A-n, 176B-n, 176C-n, etc. in each group are inputs from other cells in the array involving the same functional tasks as identified at the inputs to these AND gates, i.e., they are pairs of inputs from other cells 20 in the array 12 representing the particular positional function between neighboring cells, being part of other cell circuitry. These gates are indicated as being outside the dotted boundary of cell 20 of Figure 30.

An example of AO gate operation and particular positional function between neighboring cells is shown in Figures 31A and 31B for MOVED DOWN RIGHT NEIGHBORS in the cell array. In Figure 31A each of the nine AND gates 176I-1 to 176I-9 represent the results of pairs of inputs from diagonally positioned "down right" array cells represented by the numeral identification in Figure 31B. The cells are numbered 11, 12, 13, 14, 21, 22, 23, 24, 31, 32, 33, 34, 41, 42, 43 and 44. The possible MOVED DOWN RIGHT pixel changes would be from cell 11 to cell 22; 12 to 23; 13 to 24; 21 to 32; 22 to 33; 23 to 34; 22 to 33; 31 to 42; 32 to 43 and 33 to 44.

If there is no pixel "1" present in "old" cell positions or in the "new" pixel positions, all inputs to the AND gates 176I would be low or "0" and their outputs would all low or "0". As a result, the output at OR gate 192-9 would be low or "0". Assume that the OLD SPOT input to AND gate 176I-3 is a high or "1", a pixel "1" having been detected in cell position 13. Assume further that on the next cycle, the pixel "1" is identified as PIXEL LIGHT in cell 24. Both inputs to this gate will be high or "1". The output of AND gate 176I-3 will, therefore, be a high or "1" and the output at OR gate 192-9 would be a high or "1", indicative of MOVED DOWN RIGHT of a pixel "1" from cell 13 to cell 24.

The outputs of the nine AO gates 175 are the nine inputs to the tracker 160 shown in Figure 32. The tracker 160 is a PLA of conventionally implemented logic design for implementing combinational logic functions using AND, OR and INVERT logic. For a detail discussion of programmable logic array design, see the book, "Introduction to VLSI Systems", supra, Chapter 3, pages 79-82. The logic representation for tracker 160 is shown in Figure 33. This is a symbolic representation of the tracker conflict resolution and comprises an input latch 200, the "NOT" inverters 202, AND plane 204 and OR plane 206. Each f the circles 205 along the horizontal lines in the AND plane 204 represent inputs to AND gates in the AND plane. The functioning f each circle is AND

gate transistor and the resultant horizontal utput is productive of the 22 terms listed to the left of the OR plane 206. The circles 207 in the OR plane 206 indicate the eight outputs produced upon vertical ORing of the horizontal AND gates results. Thus, the logic function and equation can be readily determined by inspection of the AND and OR planes in Figure 33. An example is given at the bottom of Figure 33 relative to TERM DOWN HALF RIGHT HALF.

In the AND plane 204 for TERM DOWN HALF RIGHT HALF, the gate inputs for term to be responsive would equal to inverted AND inputs of NOT MOVED UP-LEFT, NOT MOVED UP, NOT MOVED UP RIGHT, NOT MOVED LEFT, NOT STAYED HERE, NOT MOVED DOWN LEFT and NOT MOVED DOWN RIGHT plus the AND f MOVED RIGHT and MOVED DOWN. Thus, one pixel in an image has moved down and another pixel has moved right, indicative of a half step DOWN RIGHT, as previously exemplified in Figure 26.

In the OR plane 206, the ORing for X RIGHT are OR gates 207 for all terms involving an X right movement, which number eight terms. For the example at hand, the output X RIGHT for tracker 160 would be TERM DOWN HALF RIGHT HALF.

In Figure 32, only the X counter 162 is shown for simplicity. The outputs X RIGHT, X HALF and X FULL from the tracker 160 and OR plane 206 are fed to a conventional latch 208 which is a quasi-static input register for X counter 162.

The symbolic logic representation for the eight state counter 162 is shown in Figure 34. The logic employed for the Y counter 164 is, of course, the same.

The three inputs, X RIGHT, X HALF and X FULL are clocked by PHI-SHORT through the input latch 208 to the inverters 210 and to the AND plane 212. Each of the circles 211 at each horizontal line of the AND plane represents an input to an AND gate, so that each circle can be characterized as an AND gate transistor. The terms for these gates are listed along each horizontal line to the right of the OR plane 214 with the listing of the binary value BA for each term.

Each horizontal line or AND gate is coupled to one r more OR gates 215 in the OR plane 214. Pairs of these OR gate outputs are inputs to the AND gates 216. The AND gate outputs are then clocked by PHI-LONG through output latch 218. The outputs of

latch 218 are quadrature signals XA, XB and XL. Signals XA and XB are the quadrature signals monitored by the user system 18. All three of these signals are fed back to input latch 208 as state feedback to the AND plane 212 and, along with tracker inputs, are productive of the terms identified in Figure 34.

Example AND plane and OR plane functions and equations are given at the bottom of Figure 34. In the AND plane 212, TERM RIGHT FULL (11) is the AND of X RIGHT, NOT X HALF, X FULL, XA and XB.

In the OR plane 214, the result for XL produced by gate 216-1 would be the ORing of all values of XX, i.e., the OR of TERM XL 1, TERM RIGHT HALF XX, and TERM LEFT HALF XX ANDed with the OR of TERM XL 0, TERM RIGHT FULL XX, TERM STAY XX, and TERM LEFT FULL XX.

The outputs XA and XB are the quadrature signals to the user system 18. These four output signals XA, XB, YA and YB provide quadrature encoding indicative of movement in a X-Y coordinate system. The phase relationship of the signals in either the X or Y direction is indicative of the direction of movement. Each of these signals is a square pulse wave. Relative to the coordinate directions identified in Figure 28, if the pulse train XA is leading in time the pulse train XB, then this means a move LEFT. If XB is leading XA, this means a move RIGHT. By the same token, if the pulse train YA is leading in time the pulse train YB, this means a move DOWN. If YB is leading YA, this means a move UP.

Up to this point, the contrasting pattern 22 under discussion has been one of light features, e.g., spots, on a dark background. Figure 35 is a representation of the circuitry for an imager 14 for sensing dark features on a light background. In previous cases, for light spot detection in a contrasting pattern 22, the cells "race" to see which will be first within its inhibition neighborhood to detect enough light and inhibit the operation of other cells in the neighborhood. The approach of the imager in Figure 35 is to see which of the cells can be last to obtain enough light. Those cells reporting out a high or "1" for SPOT DETECTED have detected a spot.

In Figure 35, the output, SENSOR NODE, of the light cells 220 are coupled to low threshold NOR gates 222. NOR gates 222 and 224 form pairs for each cell 220. The outputs of NOR gates 222 are PIXEL-LIGHT and are cross coupled to NOR gates 224

of the pair and is also an input to a respective OR gate 226 and to a respective 1 w threshold inverter 228. The output of NOR gate 224 of each NOR gate pair is cross coupled as the other input to the NOR gate 222 and the other input to the respective OR gate 226. The output of OR gates 226 is CELL DONE, and are inputs to high threshold AND gate 230, the output of which is the signal DONE to timing logic 126.

The output of the inverters 228 is the complement of PIXEL LIGHT, i.e., PIXEL DARK. All outputs, PIXEL DARK, are connected as inputs to high threshold AND gate 232, the output of which represents the signal, READY. Also, the output, PIXEL DARK-1 is an input to NOR gate 224-2, while PIXEL DARK-2 is an input to both NOR gates 224-1 and 224-3 and PIXEL DARK-3 is an input to NOR gate 224-2. NOR gate 224-2 therefore has two connected neighbors. Stable images are the outputs SPOT DETECTED.

Operation of the imager of Figure 35 is as follows. The starting states are RESET of cells with the state of SENSOR NODE high or "1", PIXEL LIGHT will be low or "0", PIXEL DARK will be at "1", SPOT DETECTED at "0" and CELL DONE at "0". SENSOR NODE will slowly go from "1" to "0" as a particular cell 220 receives light, in this case being light from the light received from the background between the dark features of a contrasting background.

Assume that SENSOR NODE-2 senses light. As a result, PIXEL LIGHT-2 will go high or "1" (both inputs to NOR gate 222-2 would be low) and PIXEL DARK-2 would be low or "0". Assume SENSOR NODE-1 remains high because it is over a dark feature. Thus, the inputs, PIXEL LIGHT -1 and PIXEL DARK-2, to NOR gate 224-1 will be both low or "0". As a result, the SPOT DETECTED-1 output of NOR gate 224-1 will go high or "1", indicating that it has "detected" a feature and pixel for cell 220-1. OR gate 226-1 (CELL DONE-1) will go high or "1" as an input to AND gate 230. CELL DONE-2 will also go high or "1" since PIXEL LIGHT-2 is high or "1". By the same token, cell 220-3 will report its CELL DONE-3 high or "1", after having either sensed light or detected a feature as just explained, respectively, relative to cells 220-1 and 220-2.

Note that when all cells have received light, it is possible for the cell array to arrive at a stable state in which no features were detected, i.e, all SPOT DETECTED are at "0" and all PIXEL LIGHT outputs are at "1". Therefore, in the case of Figure 35 comprising 3 pixel neighbor inhibiting dark spot sensors, five stable images are possible: two stable

"complete" images 101 and 010 and three stable "subset" images, 100, 001 and 000. By "subset", it is meant that the images 100 and 001 are species of the image 101 while image 000 is a species of image 010.

In Figure 36, the additional "subset" images are illustrated for a four-by-four dark spot detector arrays having the designated inhibition radius. The number of additional "subset" images for each inhibition case is given. These images are in addition to the "complete" images possible for the same inhibition radius identified in Figure 12. For example, in the case of inhibition radius 3.0, the number of possible images is the 30 "complete" images identified in Figure 12 plus the additional 13 "subset" images in Figure 36, for a total of 43 images.

An advantage of this tracking scheme is that the feature pattern of dark features on a light background need not be so closely matched to the inhibition pattern selected, since the circuit logic is willing to "wait" for features to be present before a cell "claims" to have seen one. Thus, a pseudo-random distribution of dark features, such as black dots, would be of sufficient uniformity for tracking purposes.

Claims

1. Apparatus for providing bitmap images of a relatively-movable original (10), including an array (12) of sensors (20) each capable of sensing the incidence of radiation on it, and means (72) for interconnecting the sensors whereby one sensor has sensed more than the threshold amount of radiation, it inhibits at least one adjacent sensor from responding to the incidence of further radiation on it, so that each bitmap image is made up of a pattern of responsive sensors in a field of unresponsive and/or inhibited sensors.

2. Apparatus as claimed in claim 1, wherein said sensor array may comprise either a plurality of linear arrays or a two-dimensional matrix.

3. Apparatus as claimed in claim 1 or 2, wherein said sensors and the interconnections means are integrally formed in an integrated circuit chip.

4. Apparatus as claimed in any preceding claim, including means (74) for focussing onto the array radiation from an original (10) presenting a contrasting pattern (24, 26; 28, 30).

5. Apparatus as claimed in claim 4, wherein said radiation is reflected from said contrasting pattern.

6. Apparatus as claimed in any preceding claim, in which each sensor comprises a dynamic node (36), reset means (38) coupled to said dynamic node and capable of charging said dynamic node to a voltage representing a first logic state, photosensitive means (42) coupled to said dynamic node and capable of discharging said dynamic node to a voltage representing a second logic state, logic means (46, 48) coupled to said dynamic node and capable of performing a logic NOR function, the outlet (50) said logic means being connected to the inlet of similar logic means of at least some of the other sensors in said array, whereby those other sensors are inhibited by the first sensor being changed to its second logic state.

7. Apparatus as claimed in claim 6, wherein said logic means comprises cross-coupled NOR gates (60) an inlet of one NOR gate being coupled to th outlet of one sensor, and at least one other inlet to said one NOR gate being coupled to the outlet of the other NOR gate, other inlet to said other NOR gate being coupled to the outlet of at least one other sensor.

8. Apparatus as claimed in claim 7, in which the outlet of one NOR (61) gate is coupled to an inverter (63), the outlet of said inverter being coupled to at least one other NOR gate in another of said cross-coupled NOR gate pairs.

9. Apparatus for controlling movement of a cursor in a computer display system, including a housing (108) movable independently relatively to a planar pattern (22), the housing including means (106) for irradiating the pattern and for causing the radiation from the pattern to fall on a sensor array (12), and means (72) interconnecting the sensors for identifying those sensors which are immediately adjacent to a sensor which has responded sufficiently to incident radiation.

10. Apparatus as claimed in claim 9, including means responsive to the pattern of identified sensors for generating coordinate signals corresponding to changes in the position of the housing relative to said planar pattern.

11. Apparatus as claimed in claim 10, wherein the coordinate signals are supplied to a display device to cause movement of the display cursor over the screen corresponding to movement of the housing over the pattern.

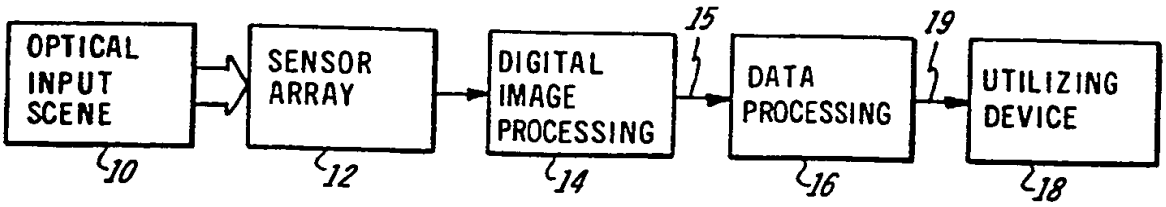

OPTICAL INPUT SCENE
10
SENSOR ARRAY
12
DIGITAL IMAGE PROCESSING
14
15
DATA PROCESSING
16
19
UTILIZING DEVICE
18

FIG. 1

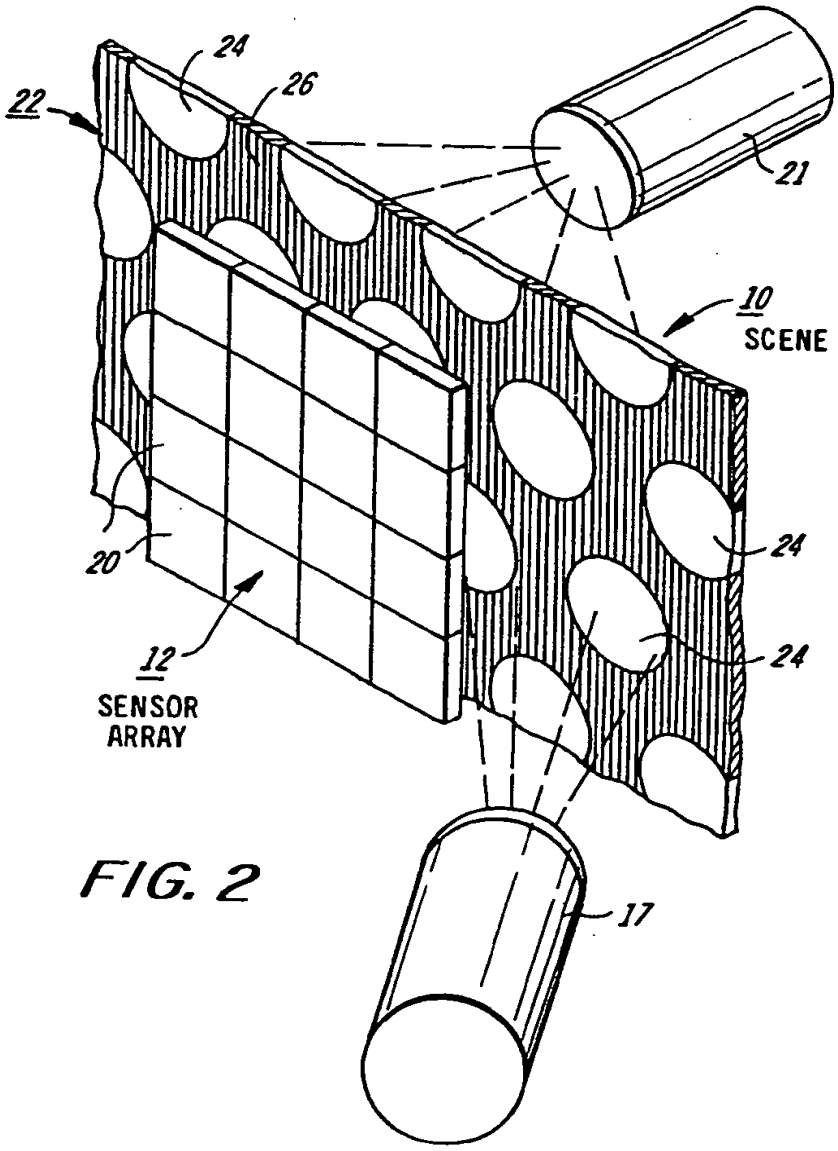

22
24
26
21
10
SCENE
20
12
SENSOR ARRAY
24
24
17

FIG. 2

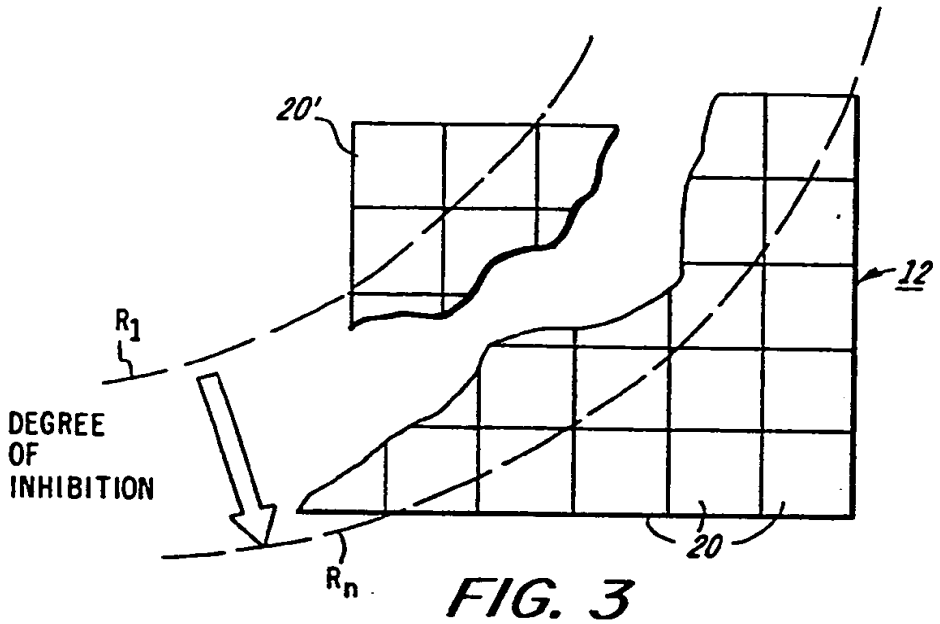


FIG. 3

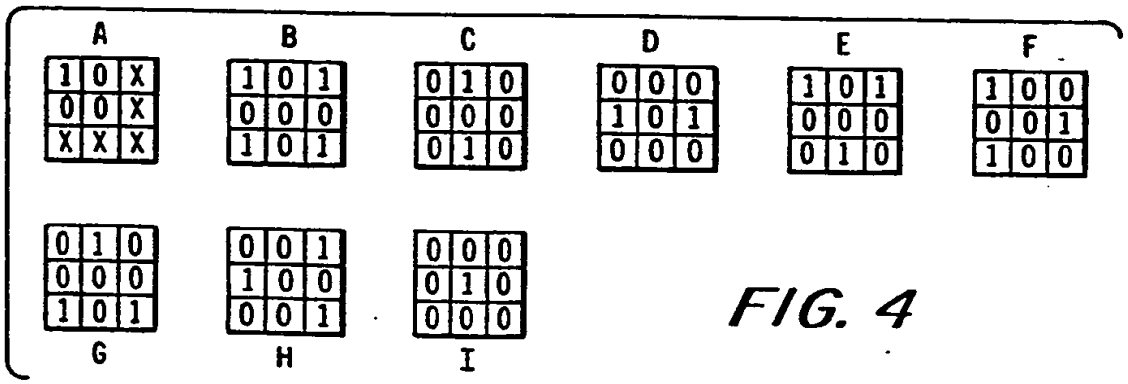


FIG. 4

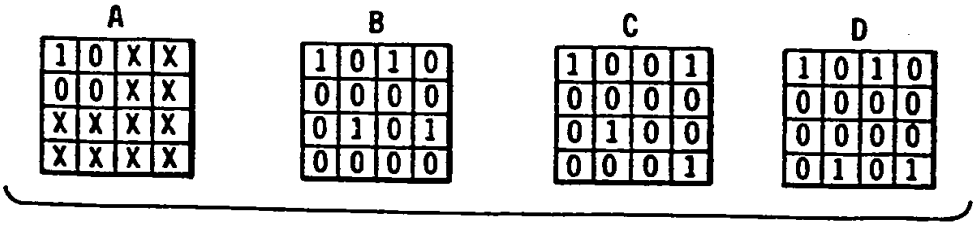


FIG. 5

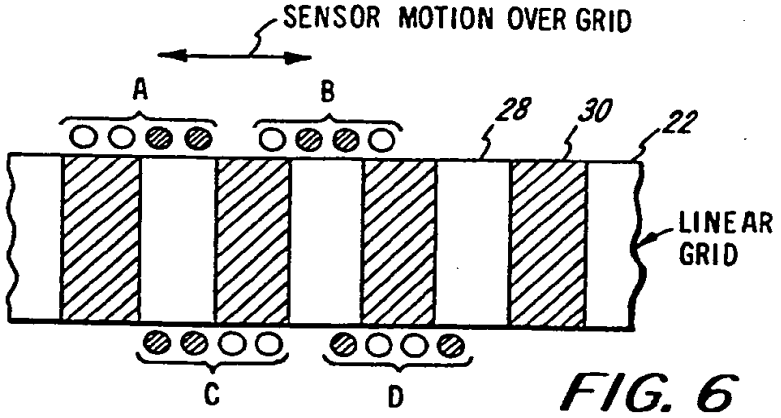


FIG. 6

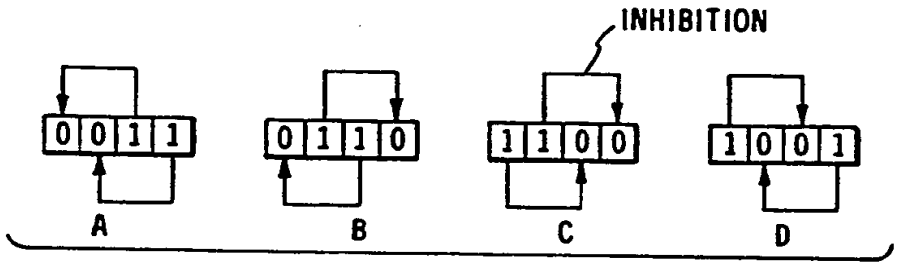


FIG. 7

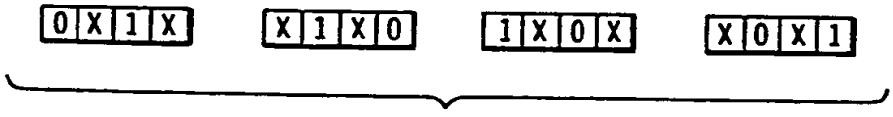


FIG. 8

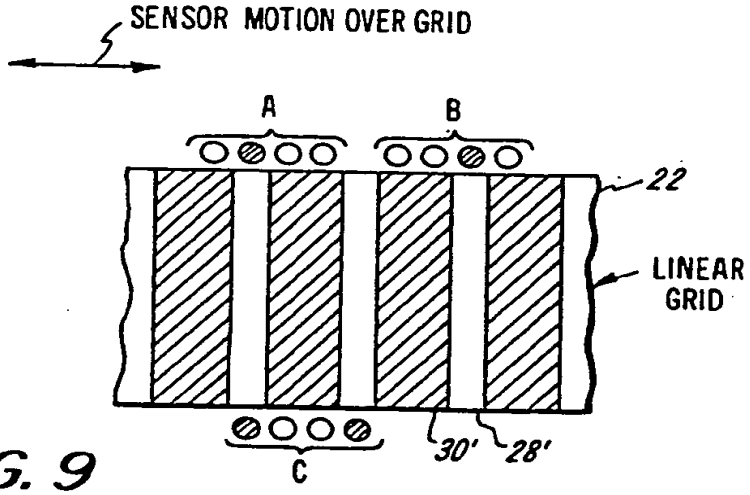


FIG. 9

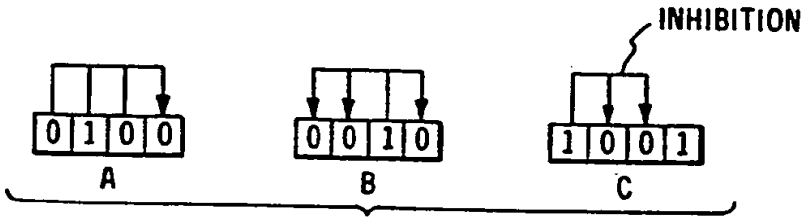


FIG. 10

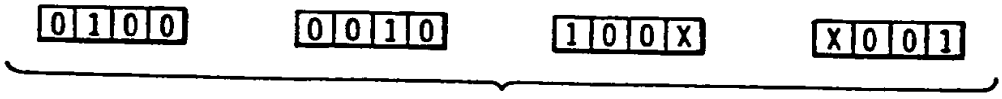


FIG. 11

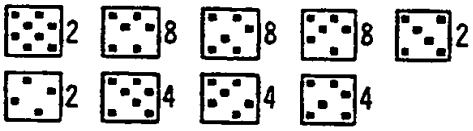
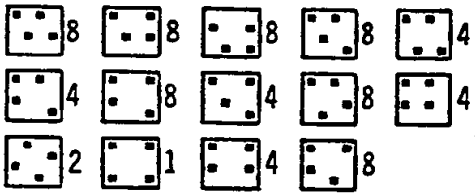
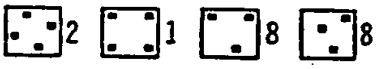
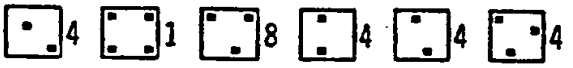
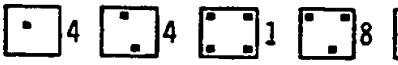
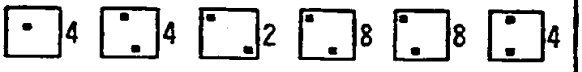
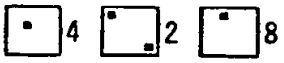
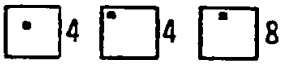
INHIBITION NEIGHBORHOODS	INHIBITION RADIUS	STABLE IMAGES AND HOW MANY OF EACH	IMAGES
	<1	1	1
	1.1	 2 8 8 8 2 2 4 4 4	42
	1.5	 8 8 8 8 4 4 8 4 8 4 2 1 4 8	79
	2.1	 2 1 8 8 4 8 4 8	43
	2.3	 4 1 8 4 4 4	25
	2.9	 4 4 1 8 4	21
	3.0	 4 4 2 8 8 4	30
	3.1	4 4 2 8 8	26
	3.2	4 2 8	14
	3.7	 4 2 8	14
	4.3	 4 4 8	16

FIG. 12

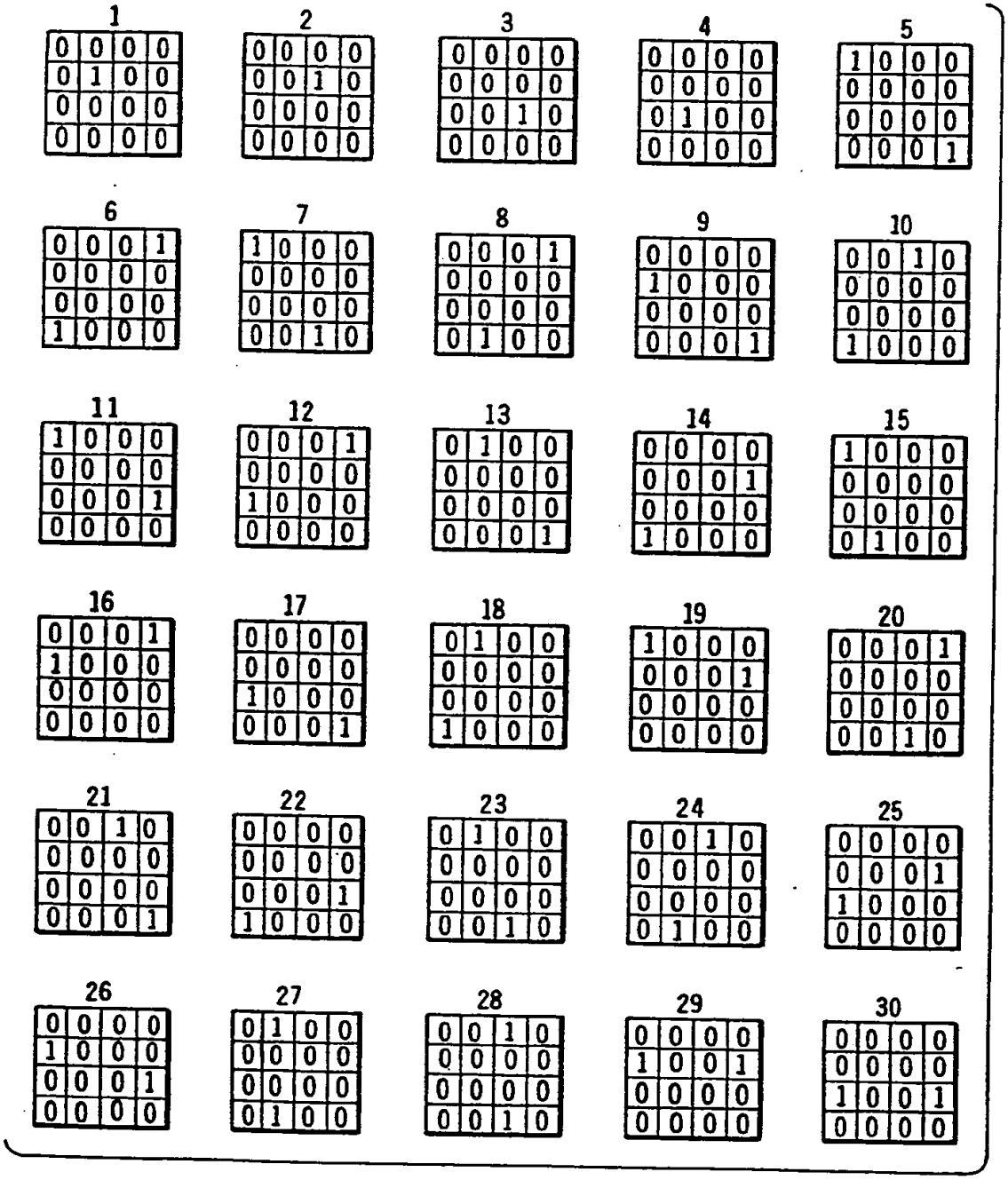

1
0 0 0 0
0 1 0 0
0 0 0 0
0 0 0 0
2
0 0 0 0
0 0 1 0
0 0 0 0
0 0 0 0
3
0 0 0 0
0 0 0 0
0 0 1 0
0 0 0 0
4
0 0 0 0
0 0 0 0
0 1 0 0
0 0 0 0
5
1 0 0 0
0 0 0 0
0 0 0 0
0 0 0 1
6
0 0 0 1
0 0 0 0
0 0 0 0
1 0 0 0
7
1 0 0 0
0 0 0 0
0 0 0 0
0 0 1 0
8
0 0 0 1
0 0 0 0
0 0 0 0
0 1 0 0
9
0 0 0 0
1 0 0 0
0 0 0 0
0 0 0 1
10
0 0 1 0
0 0 0 0
0 0 0 0
1 0 0 0
11
1 0 0 0
0 0 0 0
0 0 0 1
0 0 0 0
12
0 0 0 1
0 0 0 0
1 0 0 0
0 0 0 0
13
0 1 0 0
0 0 0 0
0 0 0 0
0 0 0 1
14
0 0 0 0
0 0 0 1
0 0 0 0
1 0 0 0
15
1 0 0 0
0 0 0 0
0 0 0 0
0 1 0 0
16
0 0 0 1
1 0 0 0
0 0 0 0
0 0 0 0
17
0 0 0 0
0 0 0 0
1 0 0 0
0 0 0 1
18
0 1 0 0
0 0 0 0
0 0 0 0
1 0 0 0
19
1 0 0 0
0 0 0 1
0 0 0 0
0 0 0 0
20
0 0 0 1
0 0 0 0
0 0 0 0
0 0 1 0
21
0 0 1 0
0 0 0 0
0 0 0 0
0 0 0 1
22
0 0 0 0
0 0 0 0
0 0 0 1
1 0 0 0
23
0 1 0 0
0 0 0 0
0 0 0 0
0 0 1 0
24
0 0 1 0
0 0 0 0
0 0 0 0
0 1 0 0
25
0 0 0 0
0 0 0 1
1 0 0 0
0 0 0 0
26
0 0 0 0
1 0 0 0
0 0 0 1
0 0 0 0
27
0 1 0 0
0 0 0 0
0 0 0 0
0 1 0 0
28
0 0 1 0
0 0 0 0
0 0 0 0
0 0 1 0
29
0 0 0 0
1 0 0 1
0 0 0 0
0 0 0 0
30
0 0 0 0
0 0 0 0
1 0 0 1
0 0 0 0

FIG. 13

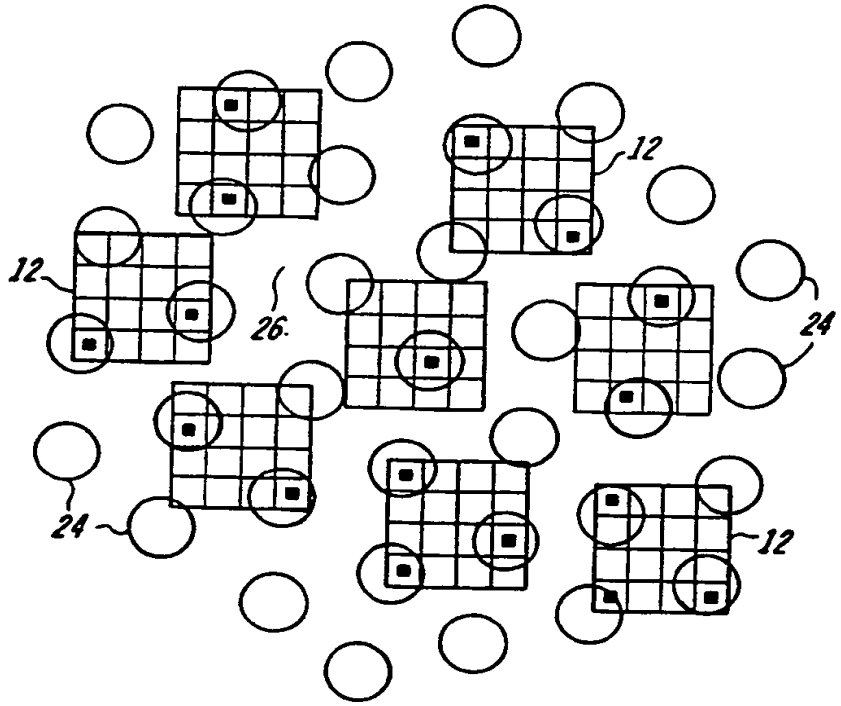


FIG. 14

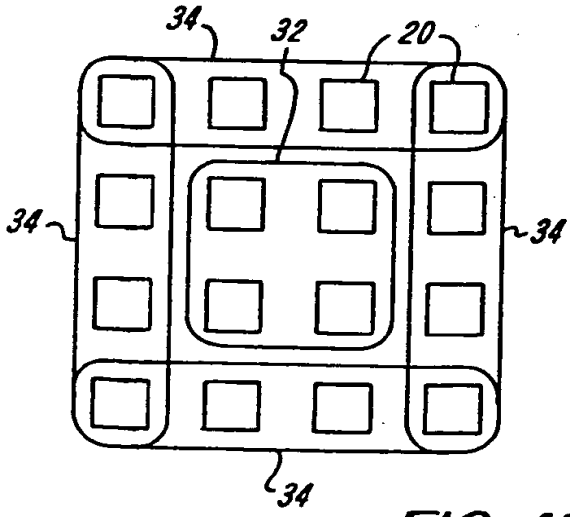


FIG. 15

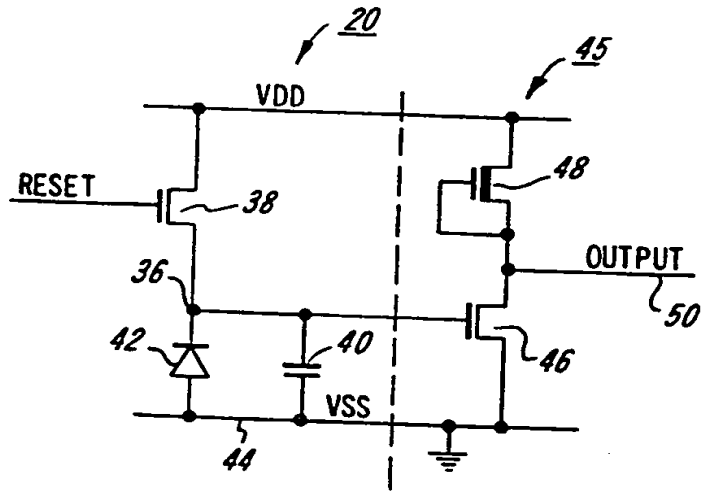

20
45
VDD
RESET
38
48
OUTPUT
50
36
42
40
46
VSS
44

FIG. 16

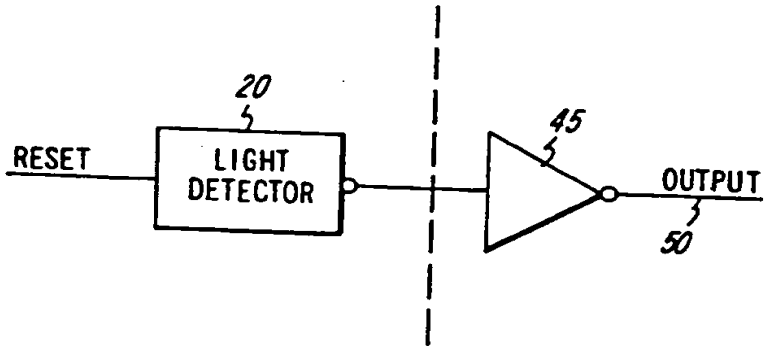

20
RESET
LIGHT
DETECTOR
45
OUTPUT
50

FIG. 17

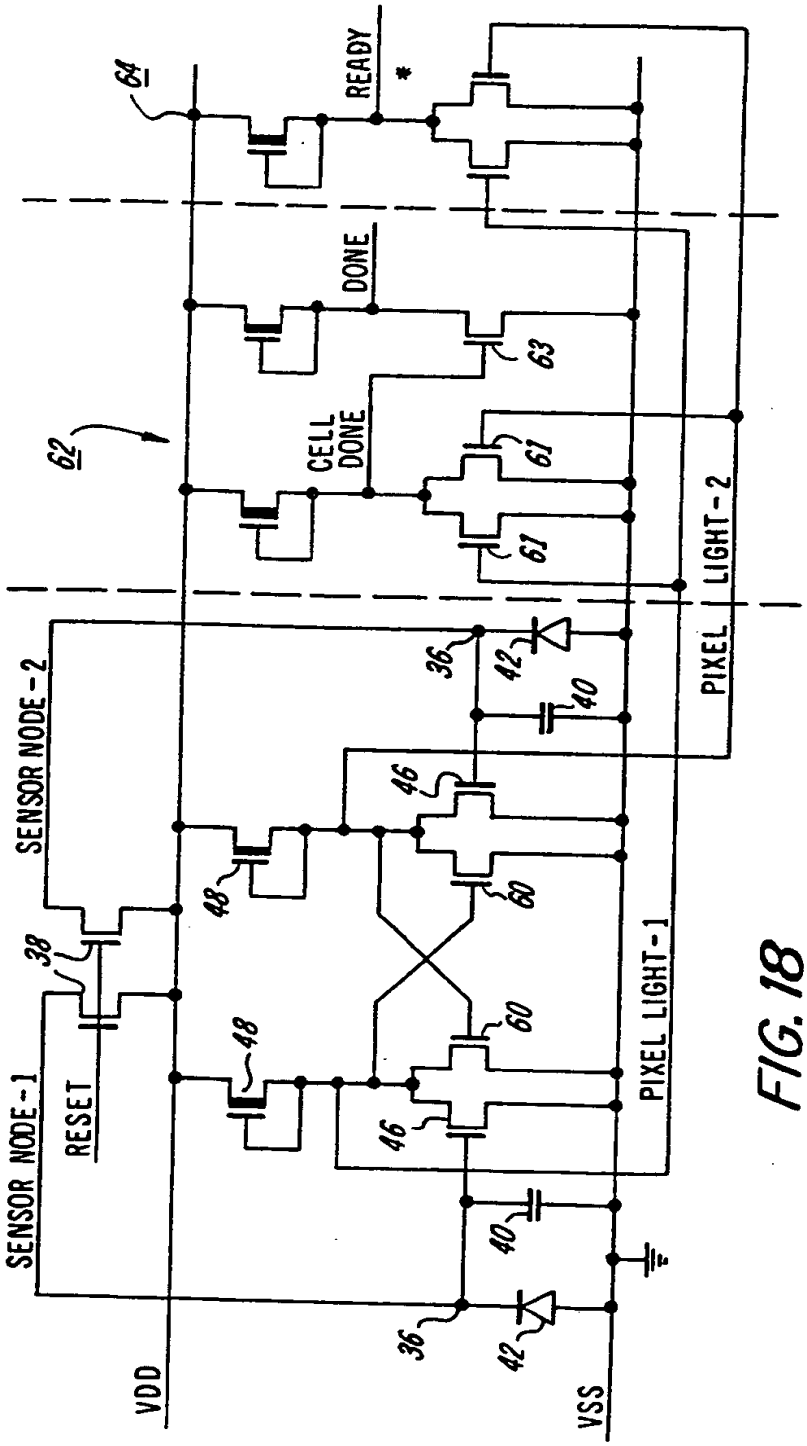

64
READY
*
DONE
63
62
CELL DONE
61
61
PIXEL LIGHT-2
36
42
40
SENSOR NODE-2
46
48
60
38
RESET
48
60
SENSOR NODE-1
46
PIXEL LIGHT-1
40
36
42
VDD
VSS

FIG. 18

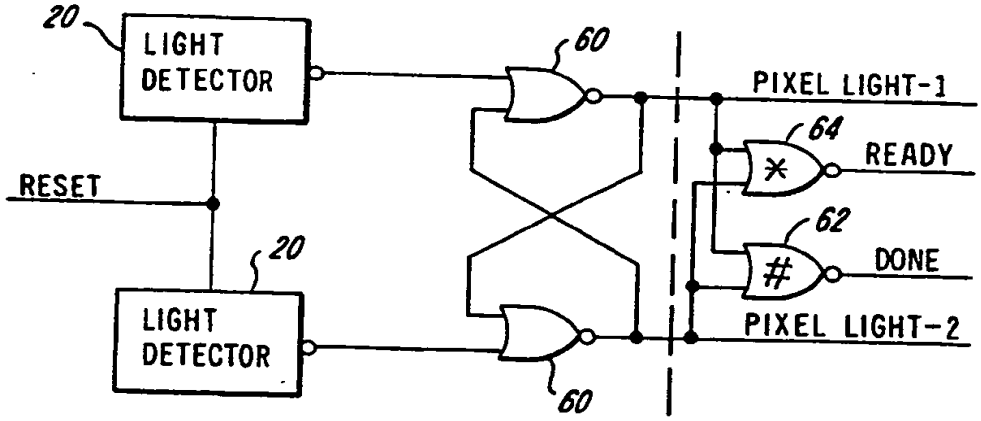

20
LIGHT DETECTOR
RESET
20
LIGHT DETECTOR
60
60
PIXEL LIGHT-1
64
READY
62
DONE
PIXEL LIGHT-2

FIG. 19

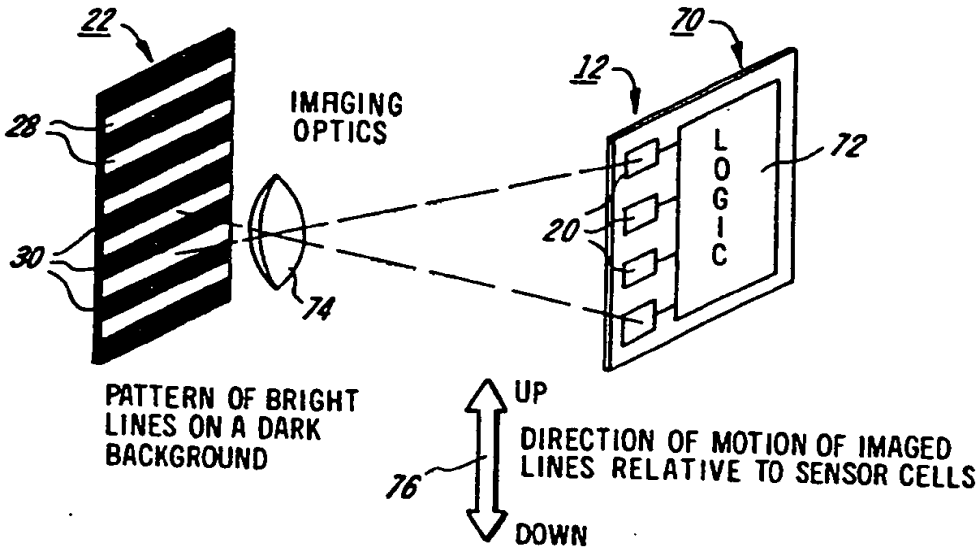

22
28
30
IMAGING OPTICS
74
70
12
LOGIC
72
20
PATTERN OF BRIGHT LINES ON A DARK BACKGROUND
76
UP
DIRECTION OF MOTION OF IMAGED LINES RELATIVE TO SENSOR CELLS
DOWN

FIG. 20

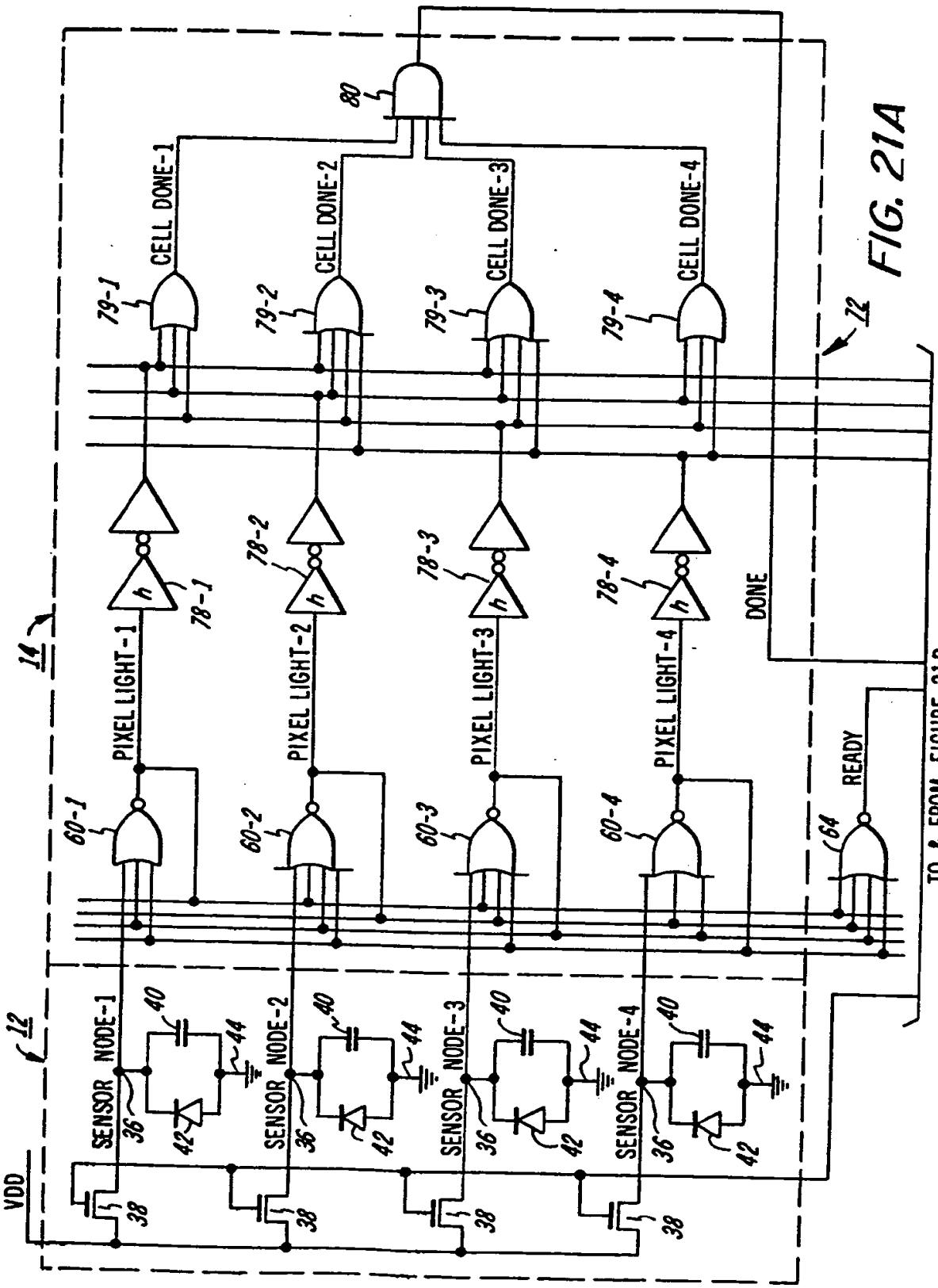

80
CELL DONE-1
CELL DONE-2
CELL DONE-3
CELL DONE-4
79-1
79-2
79-3
79-4
12
78-1
78-2
78-3
78-4
DONE
14
PIXEL LIGHT-1
PIXEL LIGHT-2
PIXEL LIGHT-3
PIXEL LIGHT-4
60-1
60-2
60-3
60-4
64
READY
TO & FROM FIGURE 21B
12
SENSOR NODE-1
SENSOR NODE-2
SENSOR NODE-3
SENSOR NODE-4
36
38
40
42
44
VDD

FIG. 21A

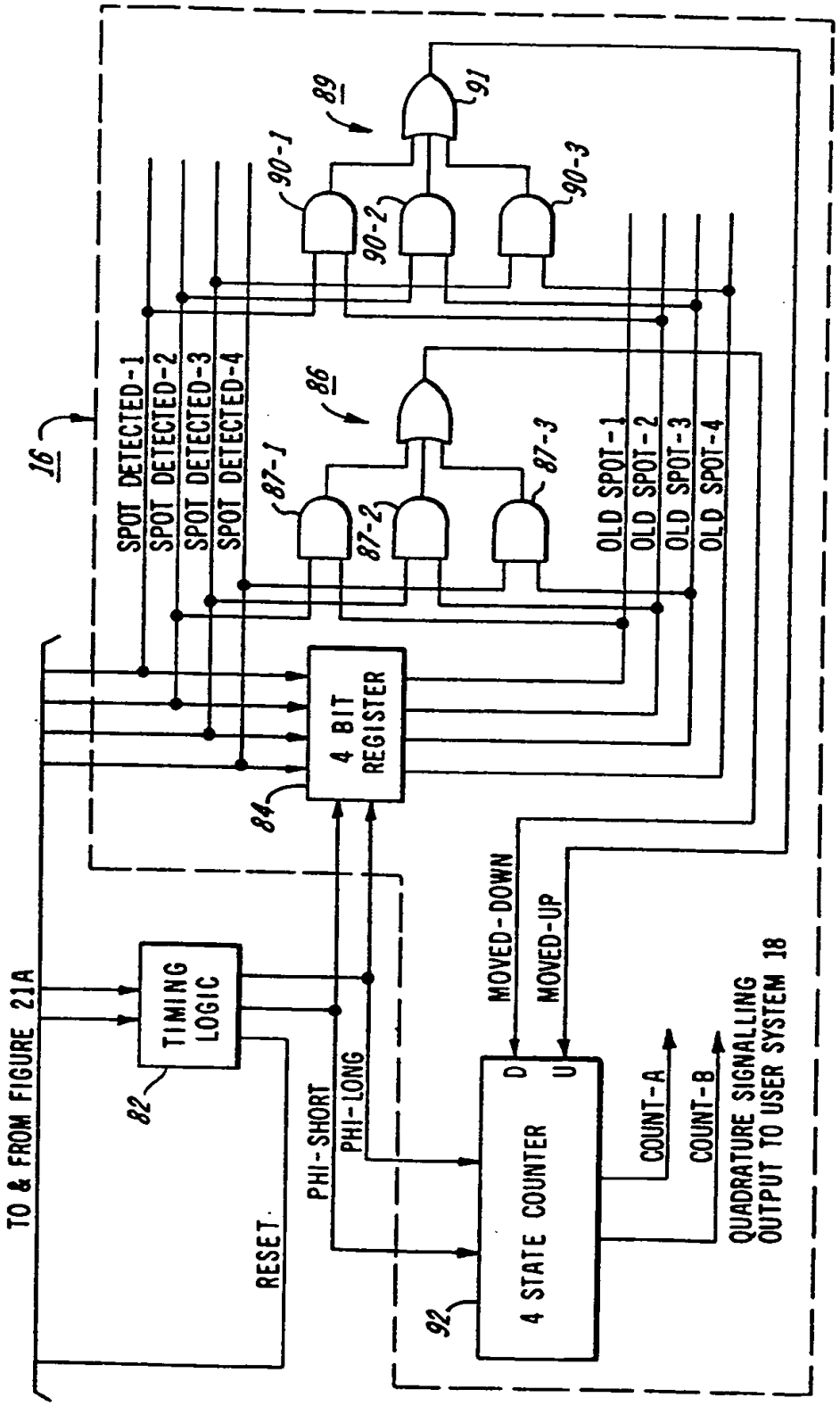

16
SPOT DETECTED-1
SPOT DETECTED-2
SPOT DETECTED-3
SPOT DETECTED-4
89
91
90-1
90-2
90-3
86
87-1
87-2
87-3
OLD SPOT-1
OLD SPOT-2
OLD SPOT-3
OLD SPOT-4
4 BIT REGISTER
84
TO & FROM FIGURE 21A
TIMING LOGIC
82
RESET
PHI-SHORT
PHI-LONG
MOVED-DOWN
MOVED-UP
D
U
4 STATE COUNTER
92
COUNT-A
COUNT-B
QUADRATURE SIGNALLING OUTPUT TO USER SYSTEM 18

FIG. 21B

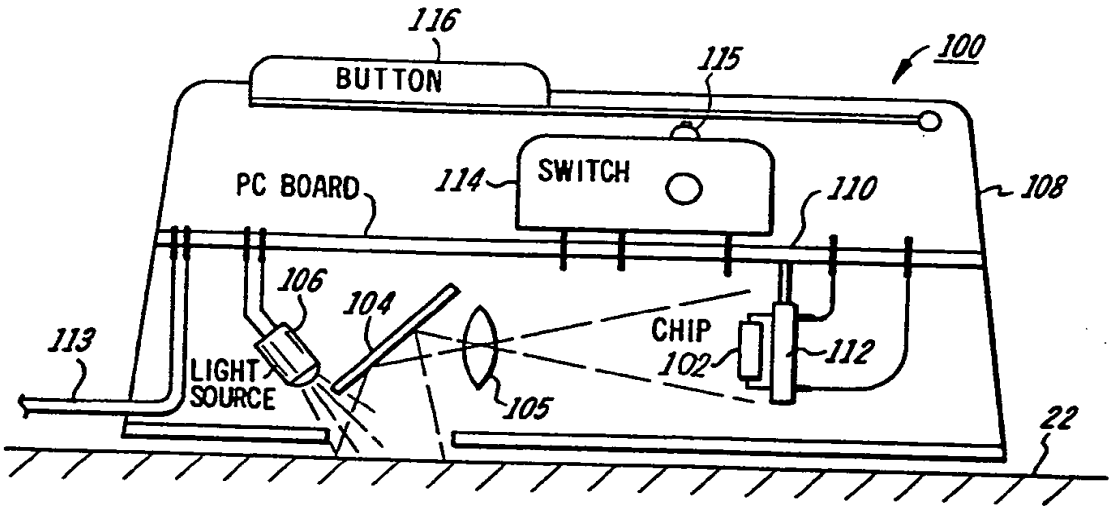

116
BUTTON
115
100
PC BOARD
114
SWITCH
110
108
106
104
113
LIGHT SOURCE
CHIP
102
112
105
22

FIG. 22

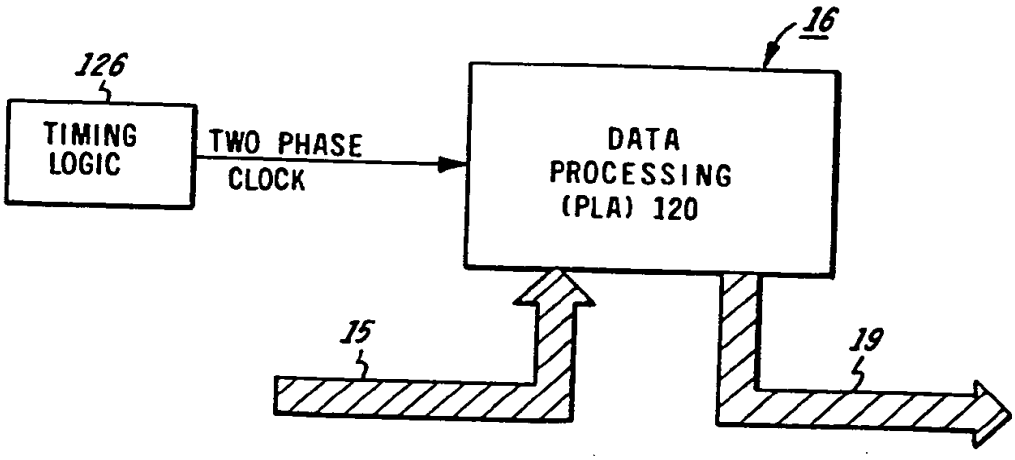

16
126
TIMING LOGIC
TWO PHASE CLOCK
DATA PROCESSING (PLA) 120
15
19

FIG. 23

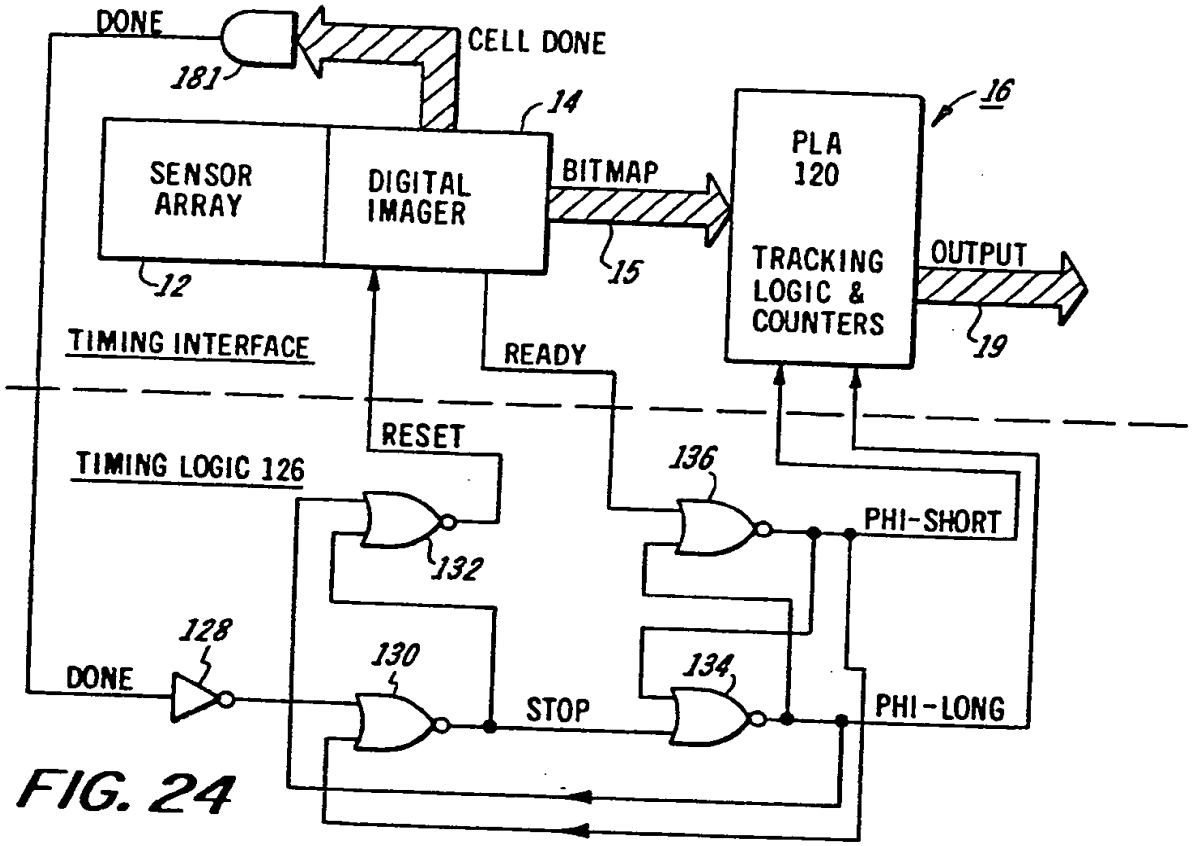

DONE
181
CELL DONE
14
16
SENSOR ARRAY
DIGITAL IMAGER
BITMAP
PLA 120
TRACKING LOGIC & COUNTERS
OUTPUT
12
15
19
TIMING INTERFACE
READY
RESET
TIMING LOGIC 126
136
PHI-SHORT
132
128
130
134
DONE
STOP
PHI-LONG

FIG. 24

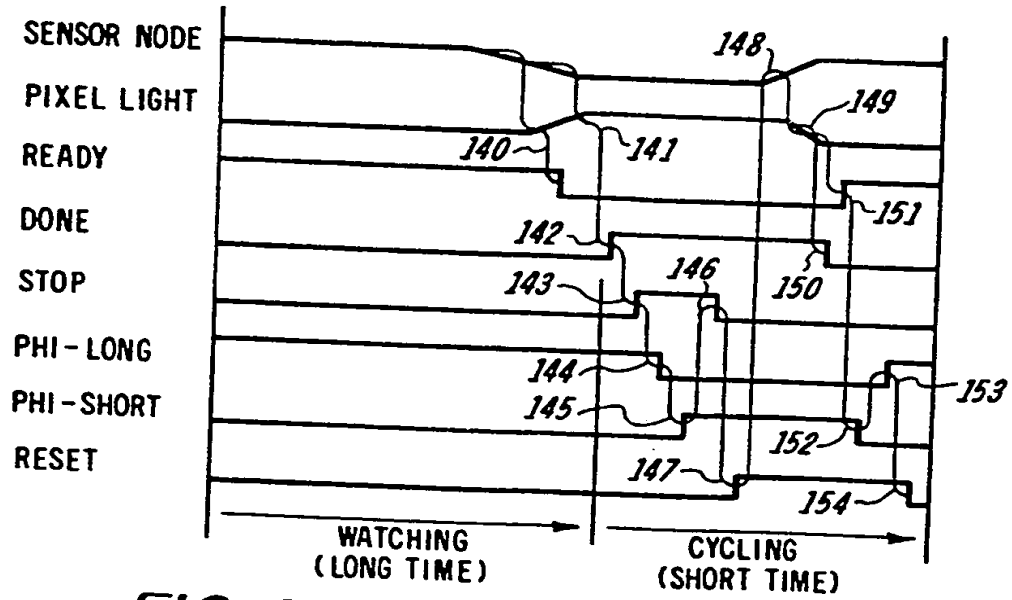

SENSOR NODE
PIXEL LIGHT
READY
DONE
STOP
PHI-LONG
PHI-SHORT
RESET
148
149
140
141
151
142
146
143
150
144
153
145
152
147
154
WATCHING (LONG TIME)
CYCLING (SHORT TIME)

FIG. 25

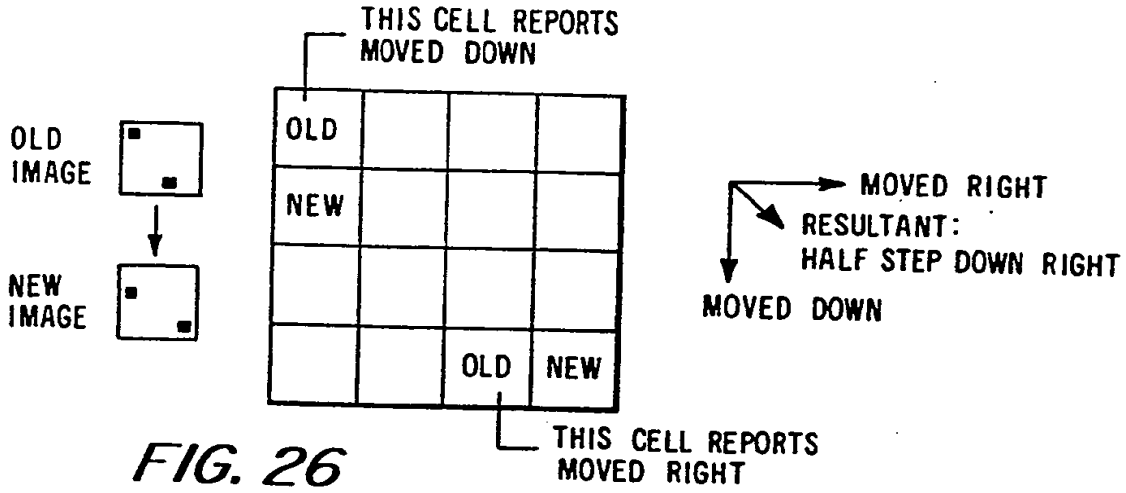

THIS CELL REPORTS
MOVED DOWN
OLD
IMAGE
NEW
IMAGE
OLD
NEW
OLD
NEW
MOVED RIGHT
RESULTANT:
HALF STEP DOWN RIGHT
MOVED DOWN
THIS CELL REPORTS
MOVED RIGHT

FIG. 26

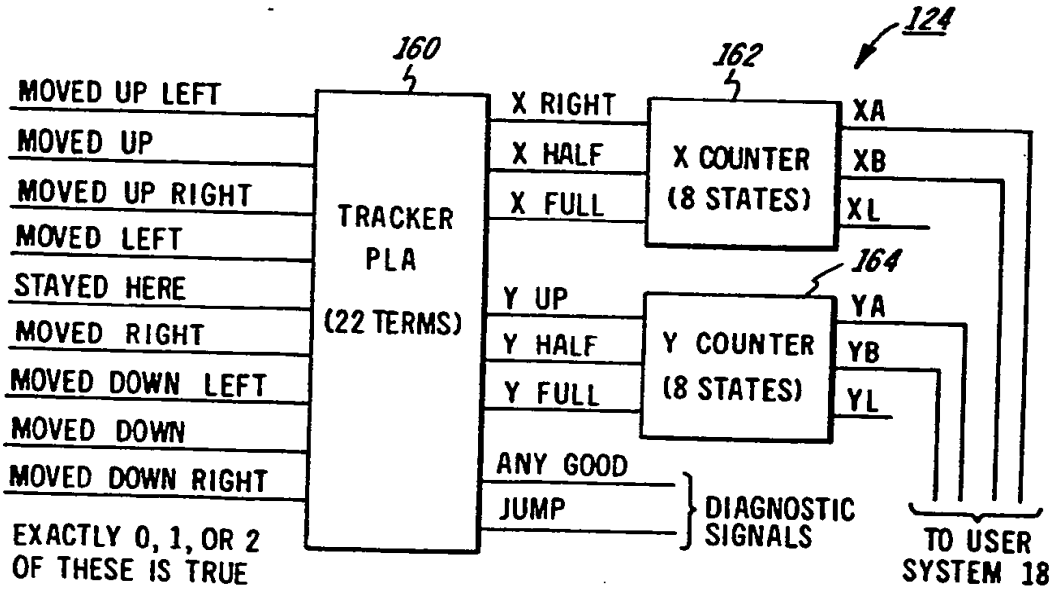

160
162
124
164
MOVED UP LEFT
MOVED UP
MOVED UP RIGHT
MOVED LEFT
STAYED HERE
MOVED RIGHT
MOVED DOWN LEFT
MOVED DOWN
MOVED DOWN RIGHT
EXACTLY 0, 1, OR 2
OF THESE IS TRUE
TRACKER
PLA
(22 TERMS)
X RIGHT
X HALF
X FULL
Y UP
Y HALF
Y FULL
ANY GOOD
JUMP
DIAGNOSTIC
SIGNALS
X COUNTER
(8 STATES)
Y COUNTER
(8 STATES)
XA
XB
XL
YA
YB
YL
TO USER
SYSTEM 18

FIG. 27

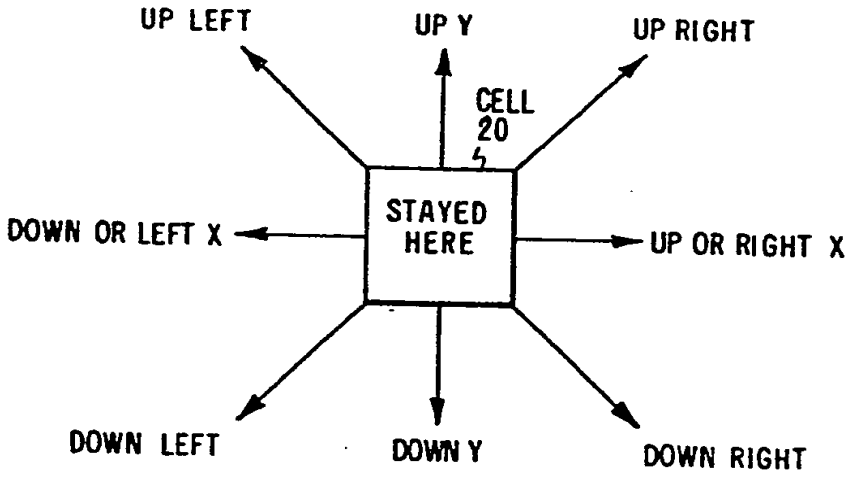

UP LEFT
UP Y
UP RIGHT
CELL
20
STAYED
HERE
DOWN OR LEFT X
UP OR RIGHT X
DOWN LEFT
DOWN Y
DOWN RIGHT

FIG. 28

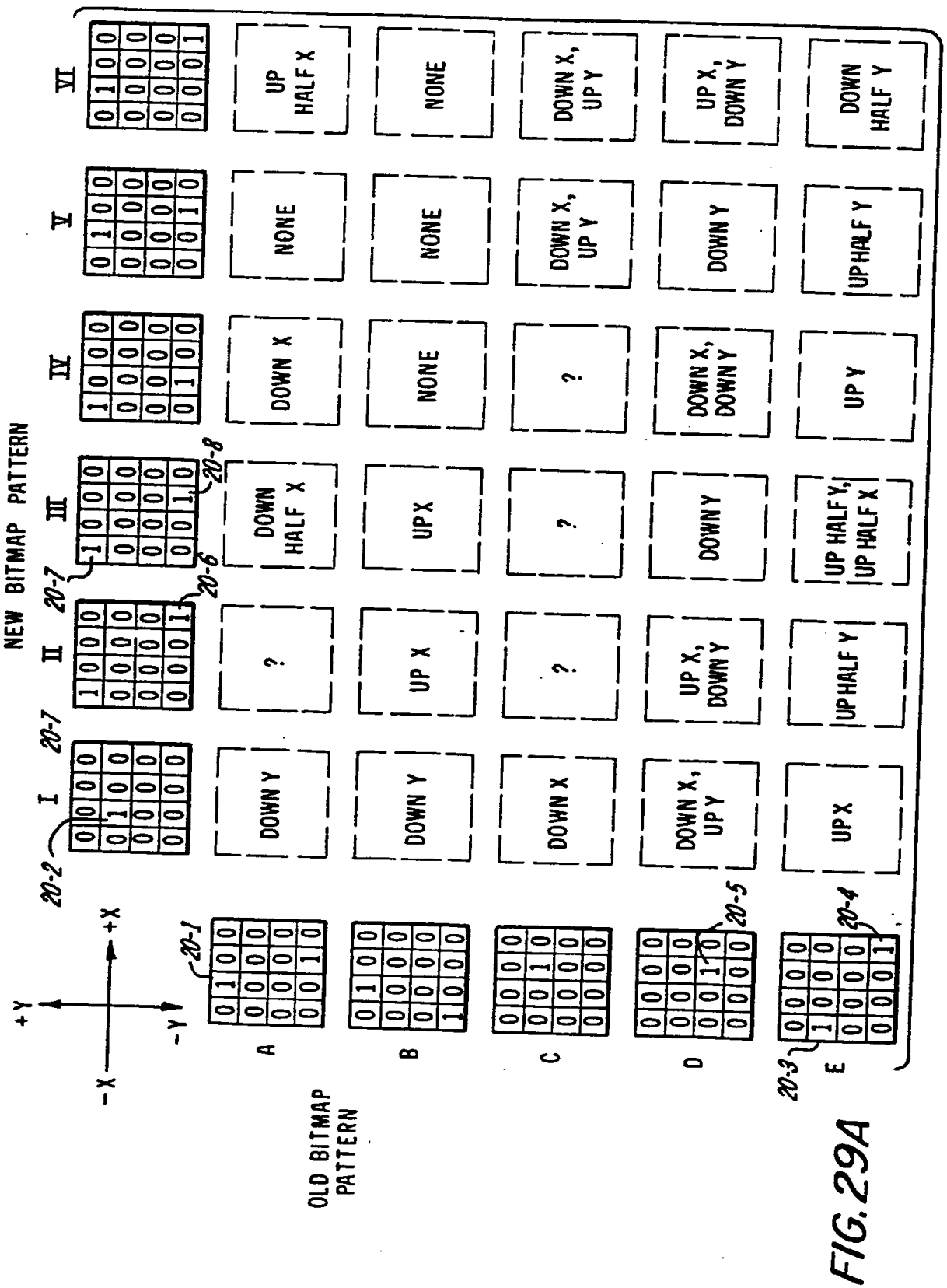
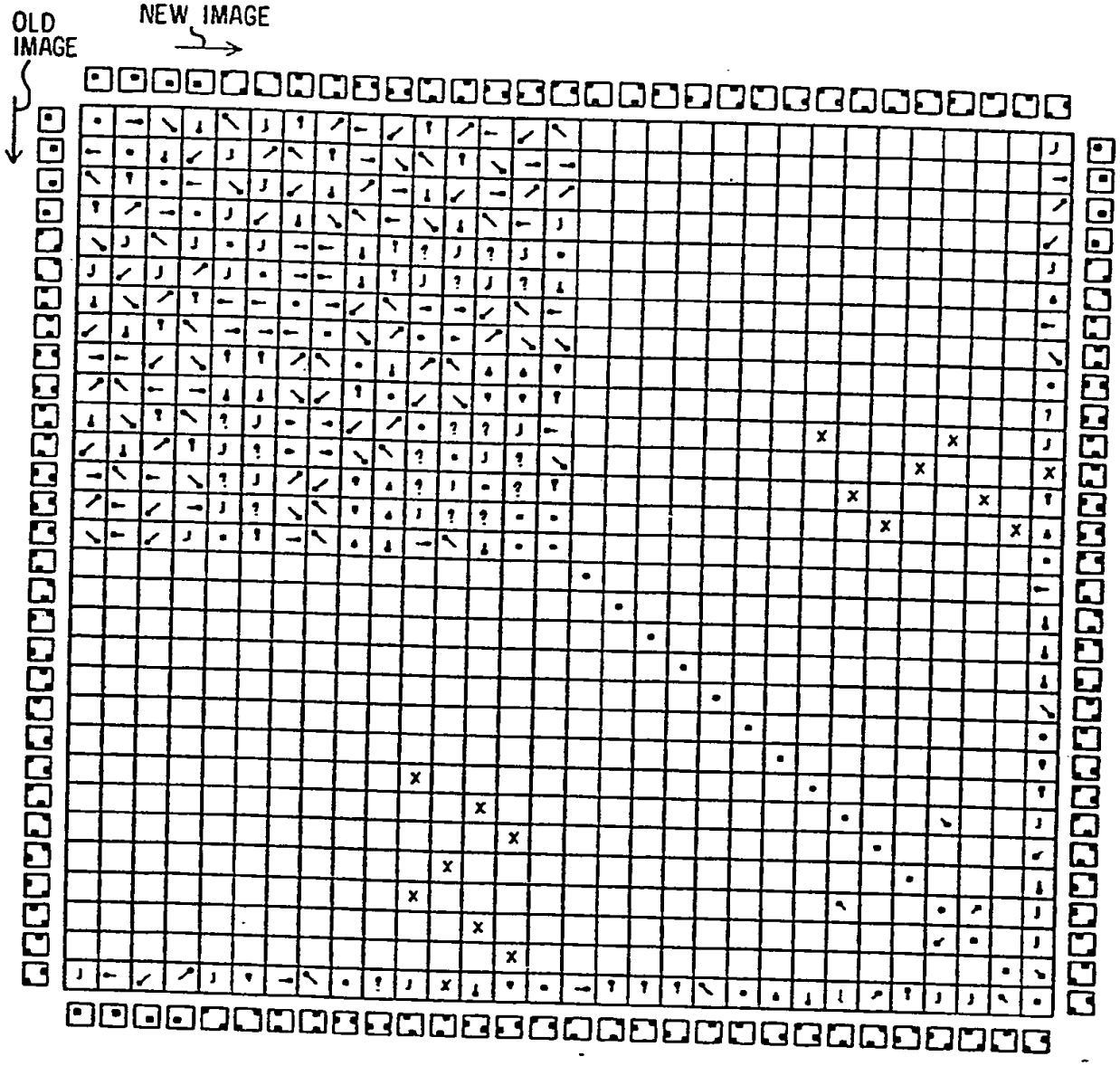

NEW BITMAP PATTERN
I
II
III
IV
V
VI
20-1
20-2
20-3
20-4
20-5
20-6
20-7
20-8
DOWN Y
DOWN Y
DOWN X
DOWN X, UP Y
UP X, DOWN Y
UP HALF Y
?
UP X
?
?
UP X, DOWN Y
UP HALF Y
DOWN HALF X
UP X
DOWN Y
DOWN Y
UP HALF Y, UP HALF X
DOWN X
NONE
NONE
?
DOWN X, DOWN Y
UP Y
UP
HALF X
NONE
DOWN X, UP Y
UP X, DOWN Y
DOWN HALF Y
+Y
-Y
+X
-X
A
B
C
D
E
OLD BITMAP PATTERN

FIG. 29A



LEGEND:

STAYED:

MOVED UP:

MOVED UP RIGHT:

STRIGHT HALF STEP: = OR

DIAGONAL HALF STEP: = OR

IMPOSSIBLE COMBINATIONS:

JUMP:

OPPOSING MOTIONS: =

ALMOST OPPOSING MOTIONS: =

FIG. 29B

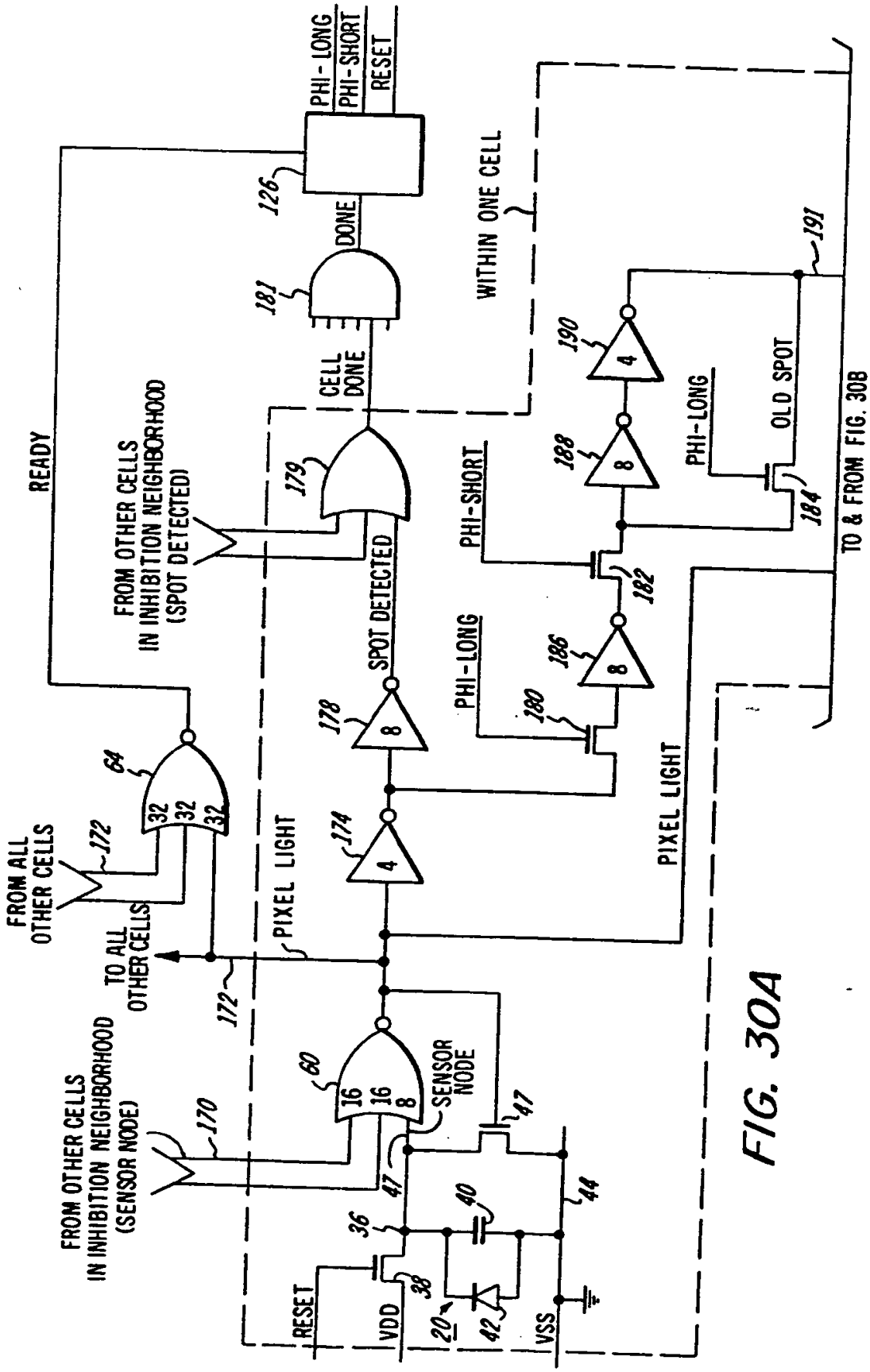

PHI-LONG
PHI-SHORT
RESET
126
DONE
181
CELL DONE
READY
WITHIN ONE CELL
191
190
4
188
8
PHI-LONG
OLD SPOT
184
FROM OTHER CELLS IN INHIBITION NEIGHBORHOOD (SPOT DETECTED)
179
SPOT DETECTED
PHI-SHORT
182
TO & FROM FIG. 30B
178
8
PHI-LONG
186
8
180
64
32
32
32
FROM ALL OTHER CELLS
172
TO ALL OTHER CELLS
PIXEL LIGHT
174
4
PIXEL LIGHT
60
16
16
8
SENSOR NODE
FROM OTHER CELLS IN INHIBITION NEIGHBORHOOD (SENSOR NODE)
170
47
47
36
40
44
RESET
VDD
38
20
42
VSS

FIG. 30A

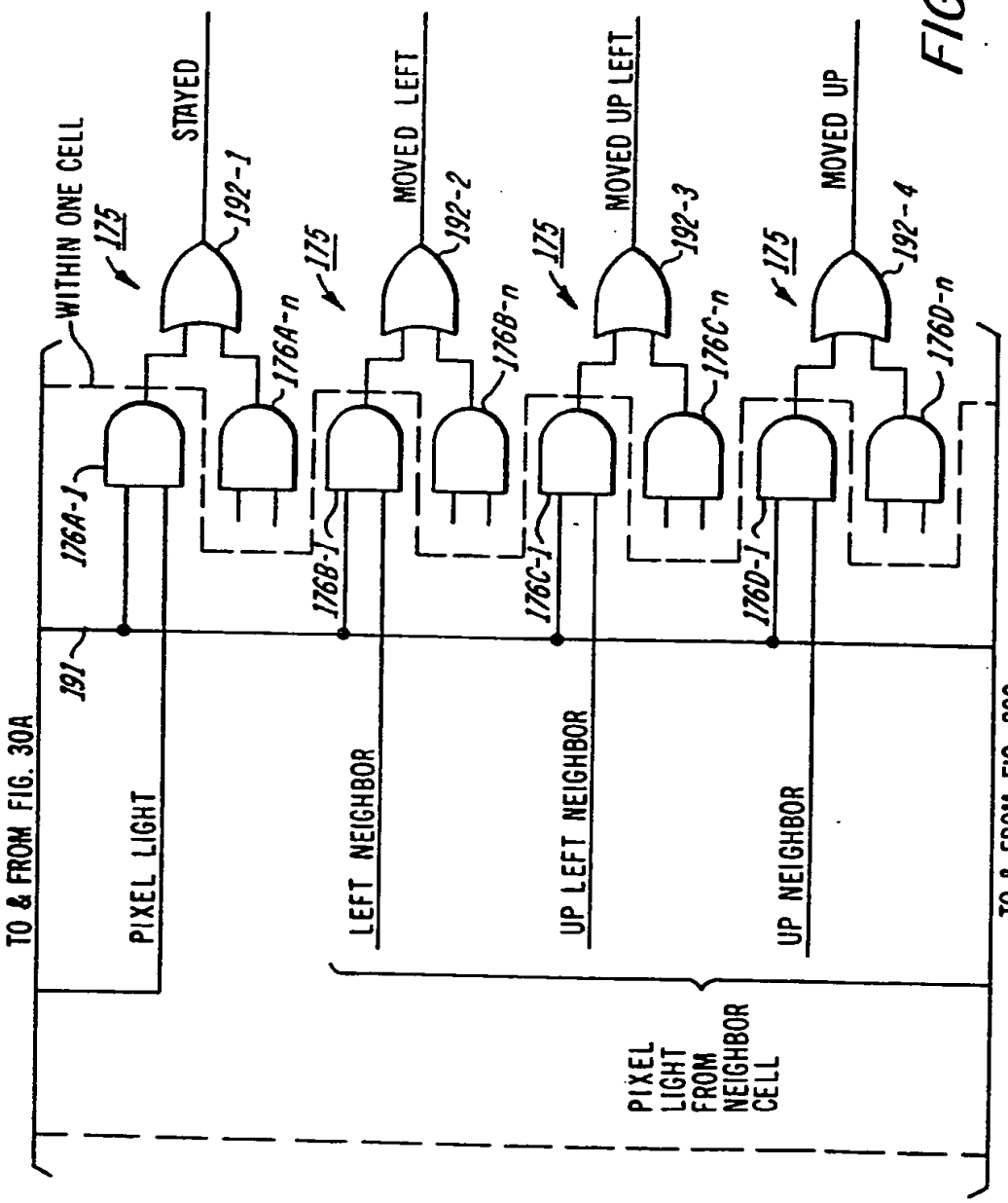

TO & FROM FIG. 30A
WITHIN ONE CELL
175
STAYED
192-1
176A-n
175
MOVED LEFT
192-2
176B-n
175
MOVED UP LEFT
192-3
176C-n
175
MOVED UP
192-4
176D-n
176A-1
176B-1
176C-1
176D-1
191
PIXEL LIGHT
LEFT NEIGHBOR
UP LEFT NEIGHBOR
UP NEIGHBOR
PIXEL LIGHT FROM NEIGHBOR CELL
TO & FROM FIG. 30C

FIG. 30B

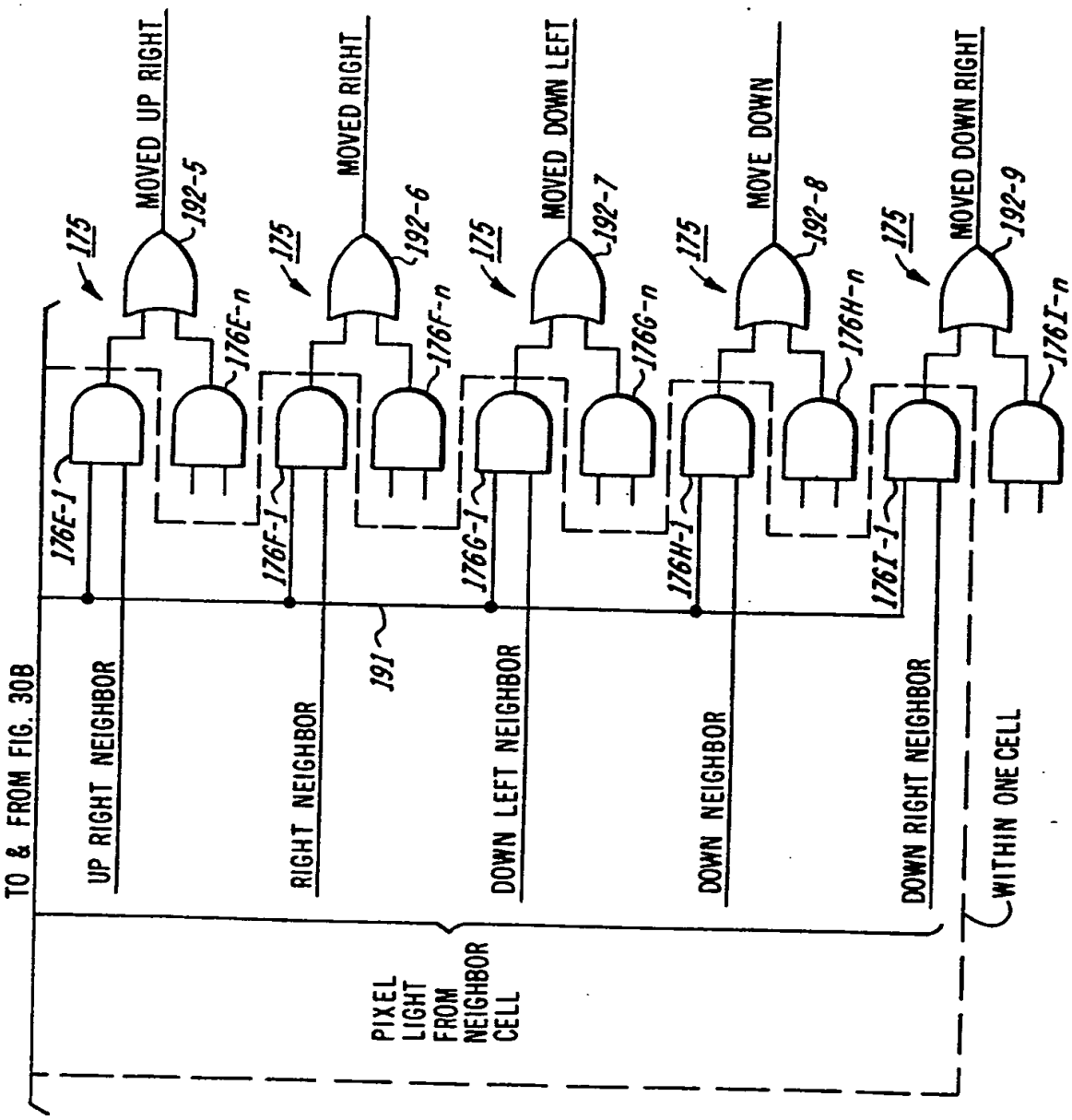

TO & FROM FIG. 30B
UP RIGHT NEIGHBOR
RIGHT NEIGHBOR
DOWN LEFT NEIGHBOR
DOWN NEIGHBOR
DOWN RIGHT NEIGHBOR
WITHIN ONE CELL
PIXEL LIGHT FROM NEIGHBOR CELL
191
175
176E-1
176E-n
176F-1
176F-n
176G-1
176G-n
176H-1
176H-n
176I-1
176I-n
MOVED UP RIGHT
192-5
MOVED RIGHT
192-6
MOVED DOWN LEFT
192-7
MOVE DOWN
192-8
MOVED DOWN RIGHT
192-9

FIG. 30C

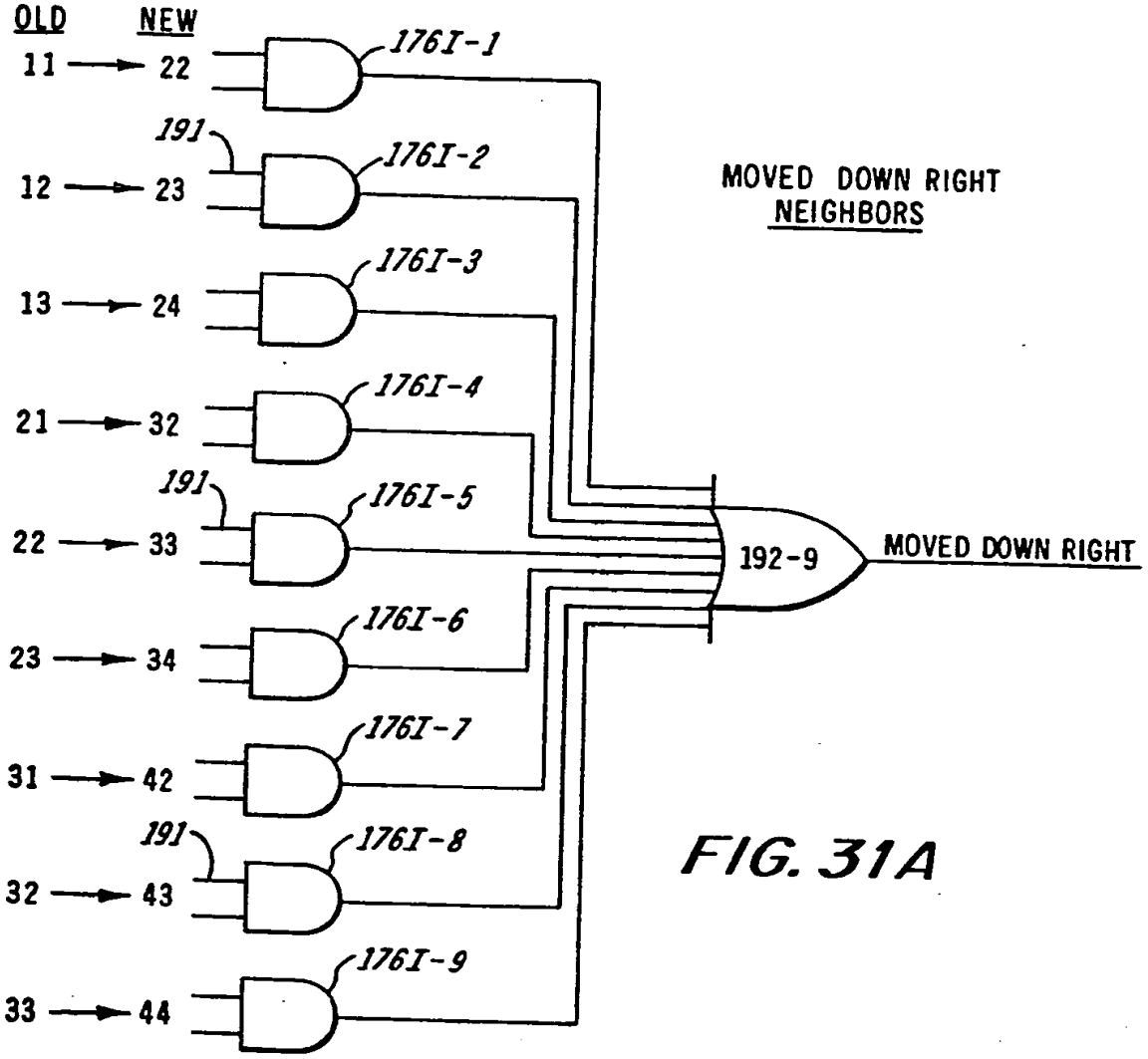


FIG. 31A

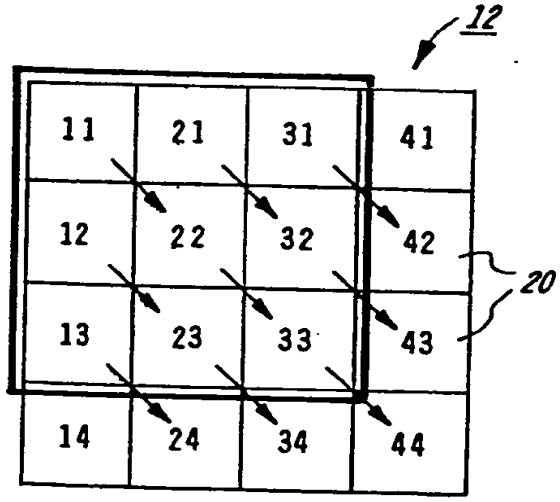


FIG. 31B

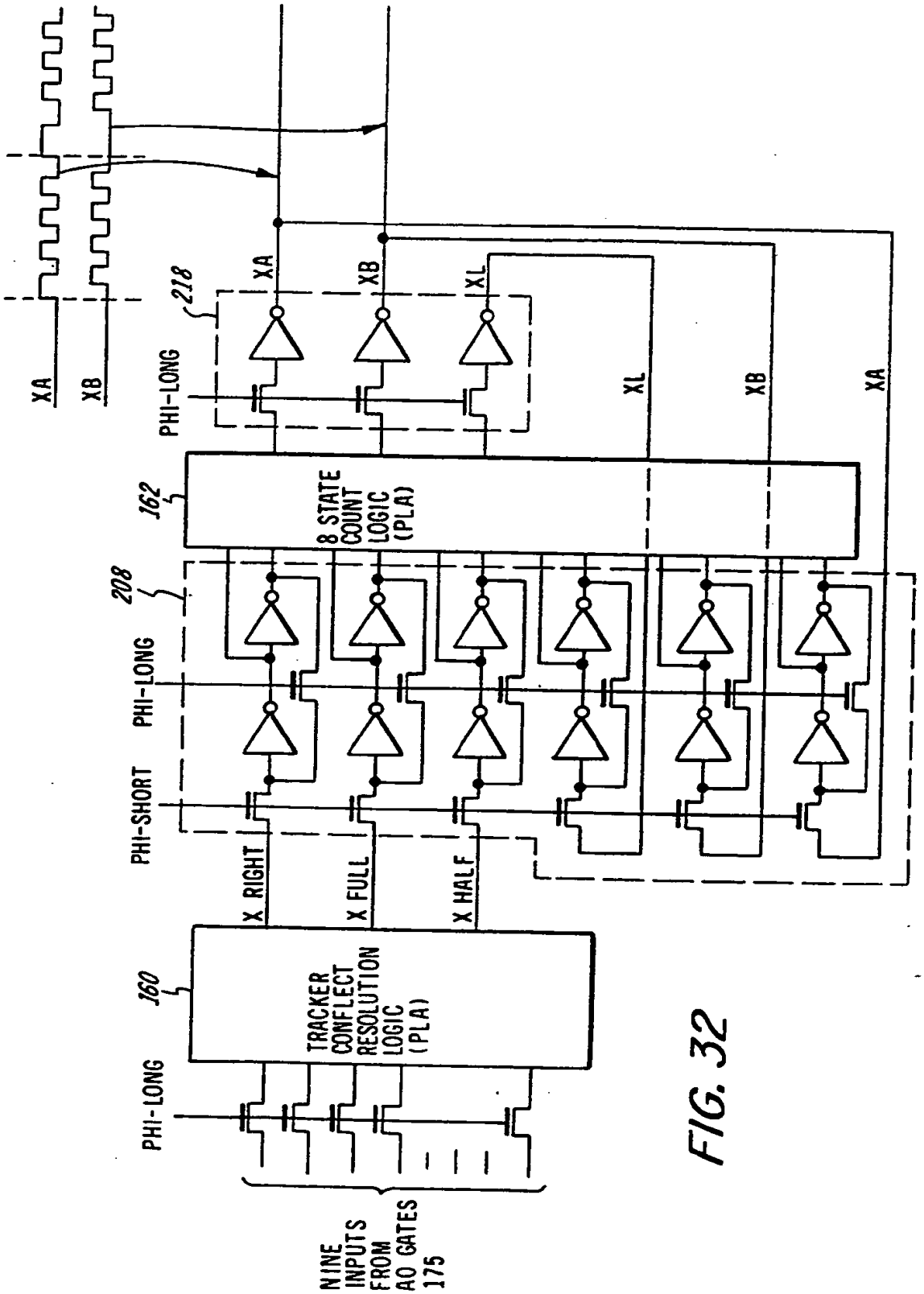

XA
XB
218
XA
XB
XL
PHI-LONG
XL
XB
XA
162
8 STATE COUNT LOGIC (PLA)
208
PHI-LONG
PHI-SHORT
X RIGHT
X FULL
X HALF
160
TRACKER CONFLECT RESOLUTION LOGIC (PLA)
PHI-LONG
NINE INPUTS FROM AO GATES 175

FIG. 32

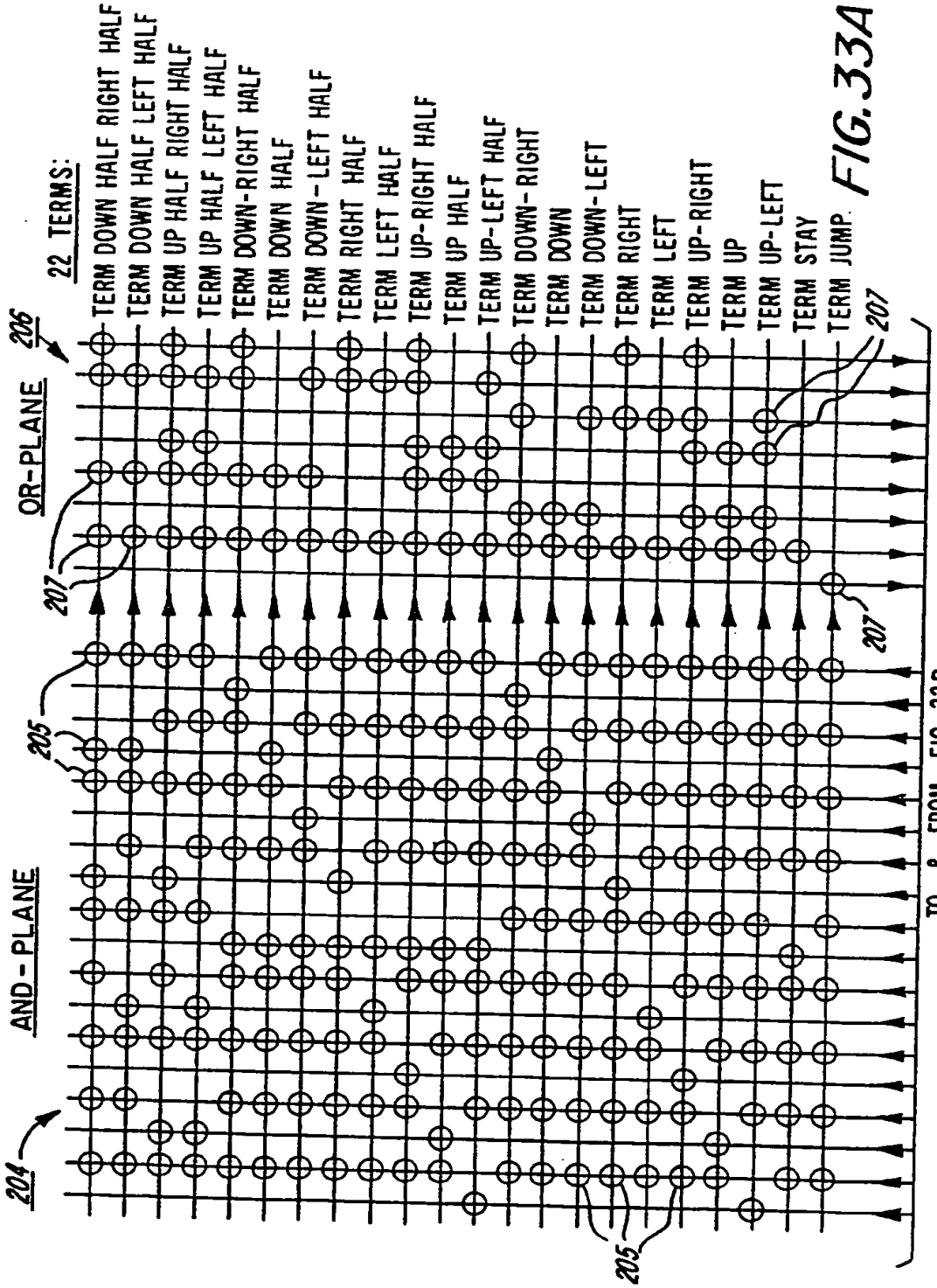
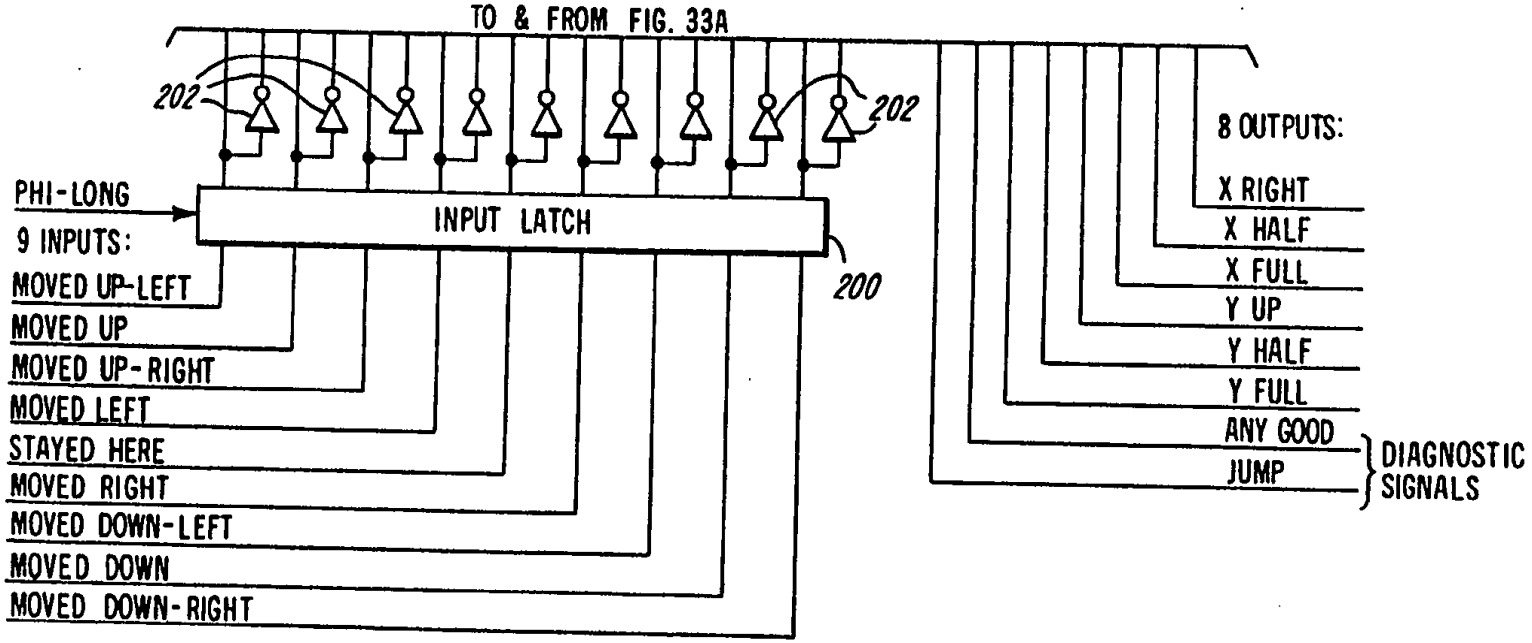

204
AND-PLANE
205
OR-PLANE
206
22 TERMS:
TERM DOWN HALF RIGHT HALF
TERM DOWN HALF LEFT HALF
TERM UP HALF RIGHT HALF
TERM UP HALF LEFT HALF
TERM DOWN-RIGHT HALF
TERM DOWN HALF
TERM DOWN-LEFT HALF
TERM RIGHT HALF
TERM LEFT HALF
TERM UP-RIGHT HALF
TERM UP HALF
TERM UP-LEFT HALF
TERM DOWN-RIGHT
TERM DOWN
TERM DOWN-LEFT
TERM RIGHT
TERM LEFT
TERM UP-RIGHT
TERM UP
TERM UP-LEFT
TERM STAY
TERM JUMP
207
207
207
205
TO & FROM FIG. 33B

FIG. 33A



EXAMPLE AND-PLANE EQUATION:
TERM DOWN HALF RIGHT HALF = (NOT MOVED UP-LEFT)
AND (NOT MOVED UP)
AND (NOT MOVED UP RIGHT)
AND (NOT MOVED LEFT)
AND (NOT STAYED HERE)
AND (MOVED RIGHT)
AND (NOT MOVED DOWN-LEFT)
AND (MOVED DOWN)
AND (NOT MOVED DOWN-RIGHT)

EXAMPLE OR-PLANE EQUATION:
X RIGHT = (TERM DOWN HALF RIGHT HALF)
OR (TERM UP HALF RIGHT HALF)
OR (TERM DOWN-RIGHT HALF)
OR (TERM RIGHT HALF)
OR (TERM UP-RIGHT HALF)
OR (TERM DOWN-RIGHT)
OR (TERM RIGHT)
OR (TERM UP-RIGHT)

FIG. 33B

0076032

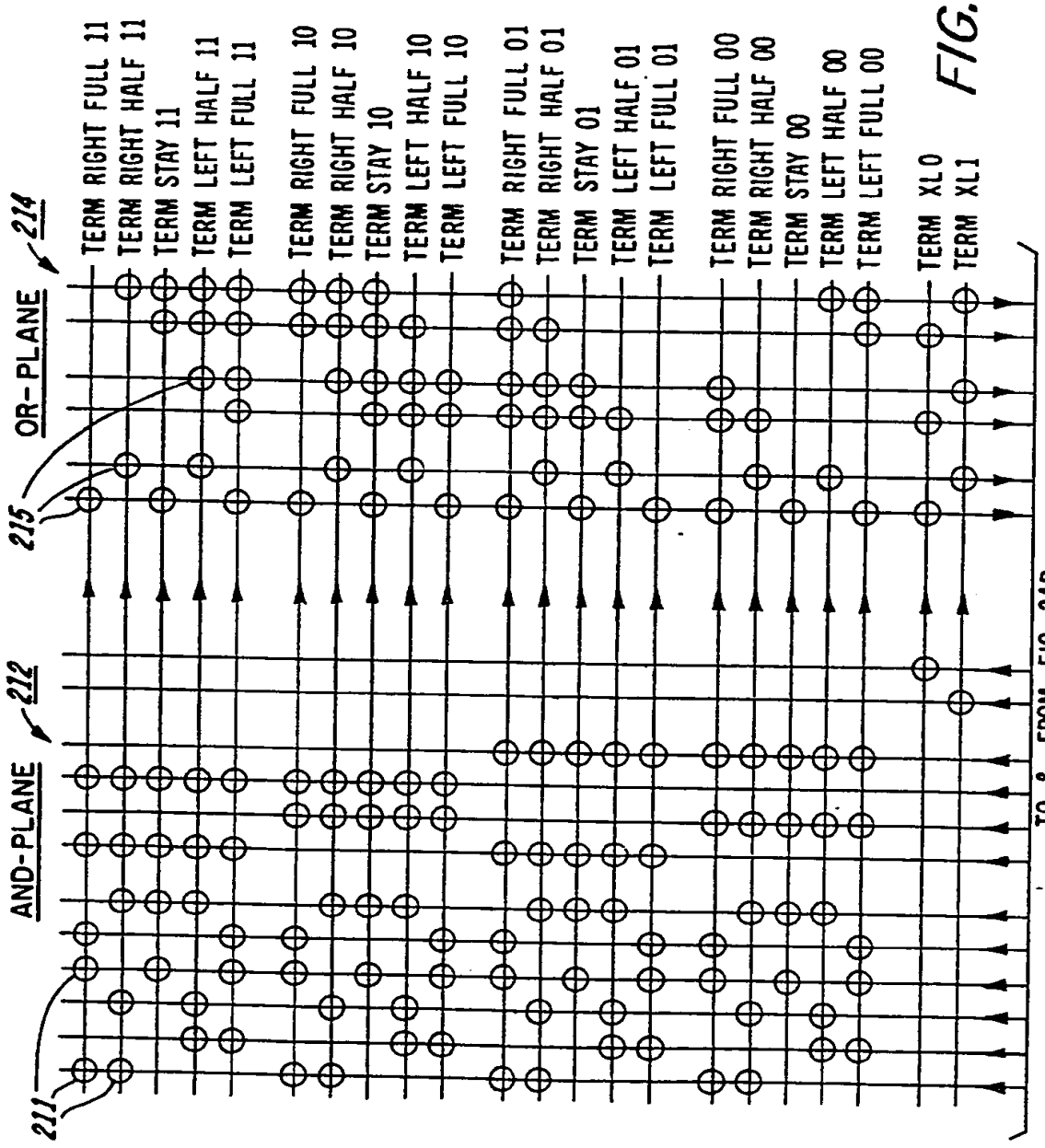
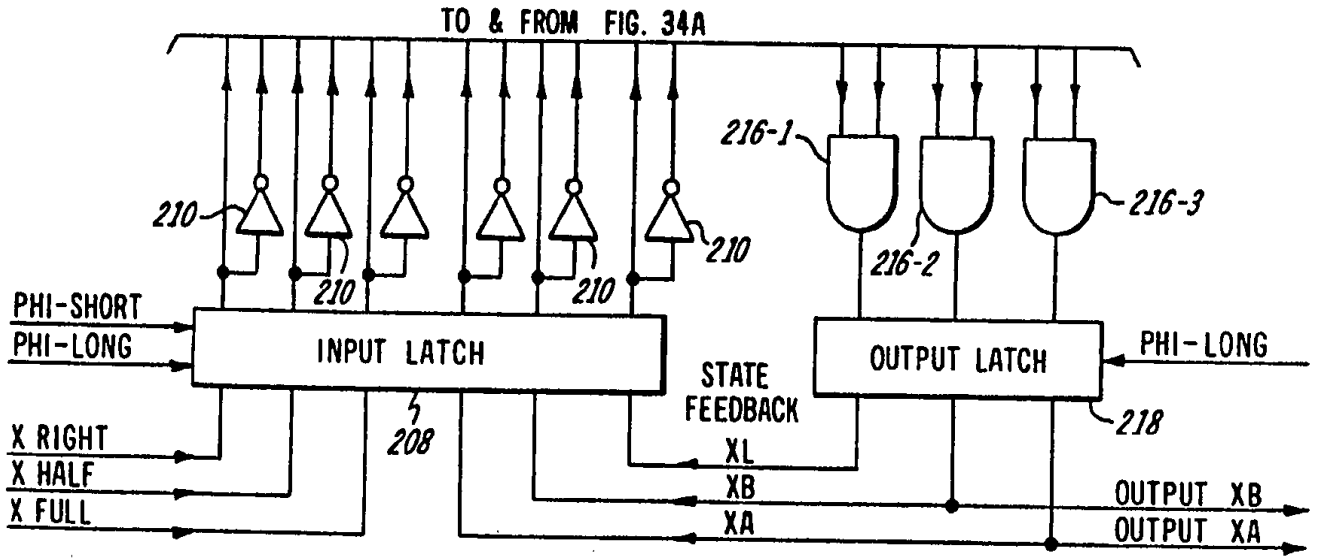

AND-PLANE
212
OR-PLANE
214
215
211
TERM RIGHT FULL 11
TERM RIGHT HALF 11
TERM STAY 11
TERM LEFT HALF 11
TERM LEFT FULL 11
TERM RIGHT FULL 10
TERM RIGHT HALF 10
TERM STAY 10
TERM LEFT HALF 10
TERM LEFT FULL 10
TERM RIGHT FULL 01
TERM RIGHT HALF 01
TERM STAY 01
TERM LEFT HALF 01
TERM LEFT FULL 01
TERM RIGHT FULL 00
TERM RIGHT HALF 00
TERM STAY 00
TERM LEFT HALF 00
TERM LEFT FULL 00
TERM XL0
TERM XL1
TO & FROM FIG. 34B

FIG. 34A



EXAMPLE AND-PLANE EQUATION:

TERM RIGHT FULL 11 = (X RIGHT)
AND (NOT X HALF)
AND (X FULL)
AND (XA)
AND (XB)

EXAMPLE OR-PLANE EQUATION:

XL = ((TERM XL1)
OR (TERM RIGHT HALF XX)
OR (TERM LEFT HALF XX))
AND ((TERM XL0)
OR (TERM RIGHT FULL XX)
OR (TERM STAY XX)
OR (TERM LEFT FULL XX))
(OR-ING TERMS FOR ALL VALUES OF XX)

FIG. 34B

0076032

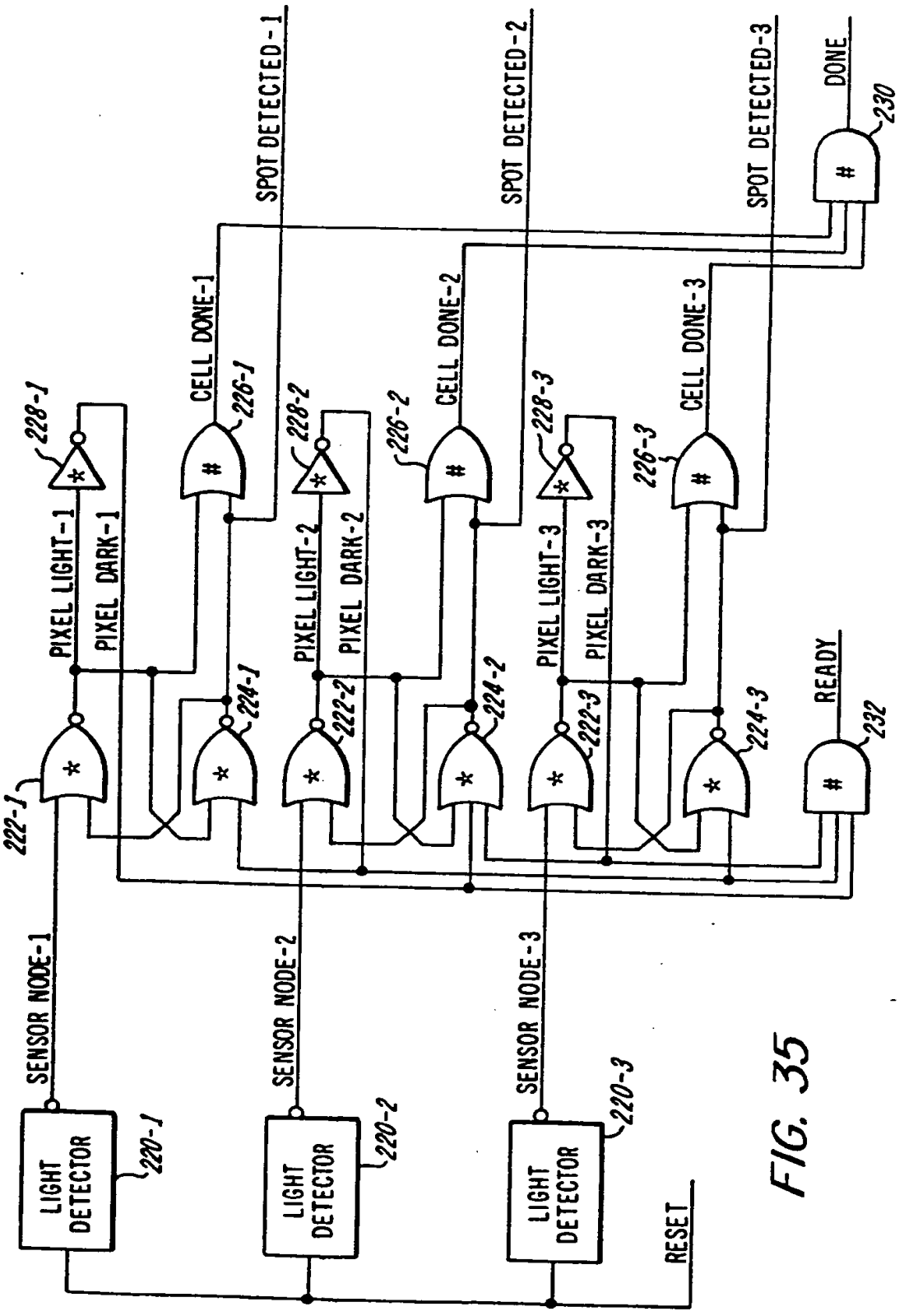

LIGHT DETECTOR
220-1
LIGHT DETECTOR
220-2
LIGHT DETECTOR
220-3
SENSOR NODE-1
SENSOR NODE-2
SENSOR NODE-3
RESET
222-1
222-2
222-3
224-1
224-2
224-3
PIXEL LIGHT-1
PIXEL DARK-1
PIXEL LIGHT-2
PIXEL DARK-2
PIXEL LIGHT-3
PIXEL DARK-3
228-1
228-2
228-3
CELL DONE-1
CELL DONE-2
CELL DONE-3
226-1
226-2
226-3
SPOT DETECTED-1
SPOT DETECTED-2
SPOT DETECTED-3
READY
232
DONE
230

FIG. 35

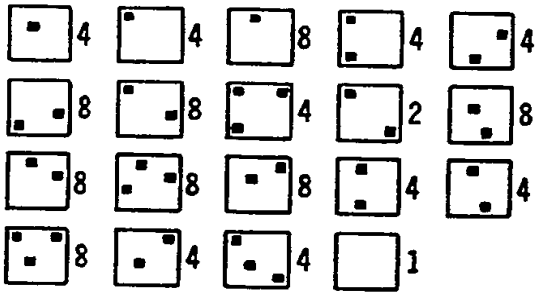
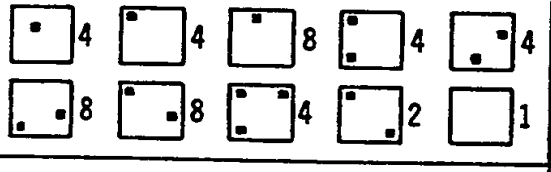
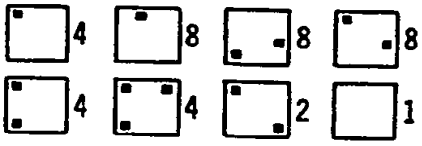
INHIBITION RADIUS	ADDITIONAL "SUBSET" IMAGES SEEN BY DARK-SPOT SENSOR ARRAY	GRAND TOTAL
2.1		146
2.3		72
* 2.9		60
3.0s		43
3.1		39

FIG. 36

(19) Eur päisches Patentamt
European Pat nt Office
Office uropéen des brevets

(11) Publication number: **0 076 032**
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(30) Priority: 28.08.81 US 296947

(43) Date of publication of application: 06.04.83 Bulletin 83/14

(84) Designated Contracting States: DE FR GB IT

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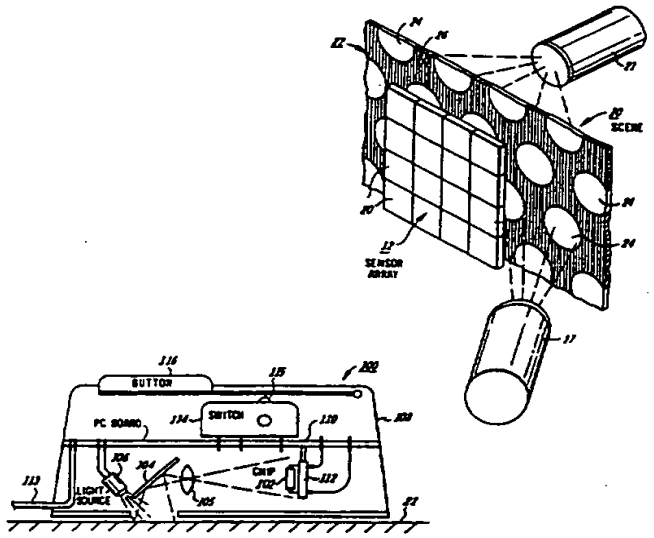
(71) Applicant: XEROX CORPORATION, Xerox Square - 020, Rochester New York 14644 (US)

(72) Inventor: Lyon, Richard F., 625 Marion Avenue, Palo Alto California 94301 (US)

(74) Representative: Weatherald, Keith Baynes et al, European Patent Attorney Rank Xerox Patent Department 338 Euston Road, London NW1 3BH (GB)

(54) Sensor arrays.

(57) A sensor array (12) provides a plurality of distinguishable bitmap images of a pattern (22) and comprises an array of sensor cells (20) capable of sensing radiation. The cells are connected in a manner to form distinguishable bitmap images of a contrasting pattern through a pattern of correspondence among the cells. Each bitmap image formed comprises a combination of one or more cells which have responded to the incidence of radiation within a field of array cells that have either not responded or been inhibited from responding. The pattern of correspondence may be one of inhibition or of response of sensors. The patterns of correspondence create bitmap images. The variations between successive bitmap images give a measure of the direction and amount of movement of the sensory array relative to the pattern, which can be used to control the movement of a cursor over a computer display screen.



EP 0 076 032 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application number: 007603

EP 82 30 4402

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
X	US-A-3 473 036 (MARCUS) * Column 1, lines 63-72; column 3, lines 59-62; column 6, lines 67-73; figure 11 *	1	G 06 K 11/06 G 06 F 3/033
A	MICROELECTRONICS JOURNAL, vol. 10, no. 1, May/June 1979, pages 35-44, Luton, G.B. C. TASSELL et al.: "Photodiode arrays-characteristics and applications" * Figure 10 *	6	
D,A	US-A-3 541 541 (ENGELBART) * Whole document *	9-11	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 13, no. 9, February 1981, page 2620, New York, USA B.E. BLISS et al.: "Ball-joint position transducers" * Whole document *	9-11	TECHNICAL FIELDS SEARCHED (Int. Cl. ³) G 06 K
A	US-A-3 701 095 (YAMAGUCHI et al.)		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-08-1983	BEINDORFF W.H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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